

# Yukon Block Diagram

Project code: 91.4BC01.001  
PCB P/N : 48.4BC01.0SA  
REVISION : 08226-SA

## PCB Layer Stackup

L1: Signal 1  
L2: VCC  
L3: Inner Signal 2  
L4: Inner Signal 3  
L5: GND  
L6: Signal 4

## CPU V\_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

## SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

## SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

## SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

## SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

## SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

## Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
**BLOCK DIAGRAM**

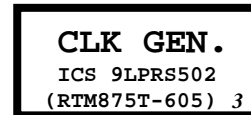
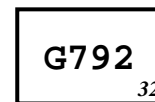
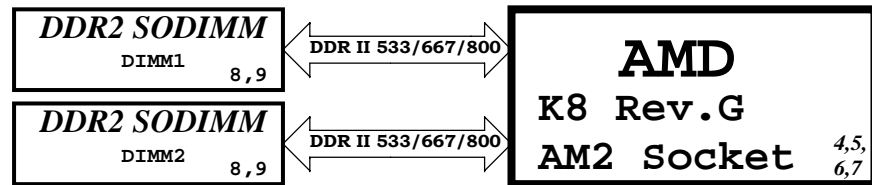
Size A3 Document Number

**Yukon**

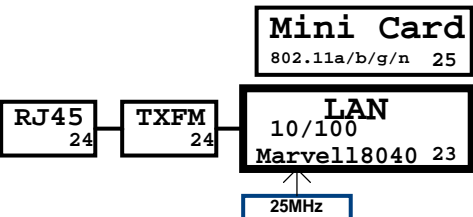
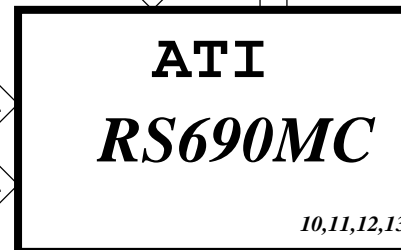
Date: Thursday, July 03, 2008

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Rev  
SA

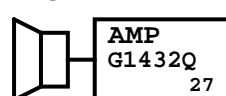
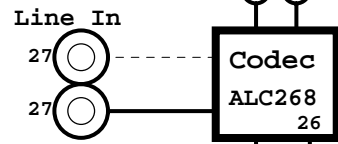


HyperTransport 16x16

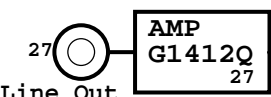


25MHz

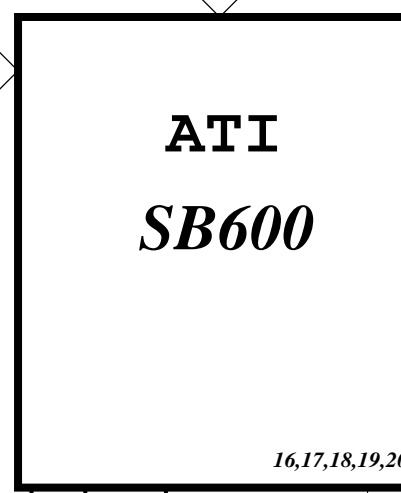
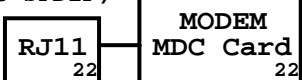
INT. MIC Array



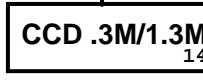
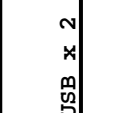
INT. SPKR



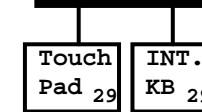
Line Out (No-SPDIF)



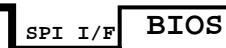
16,17,18,19,20



32.768KHz



LPC BUS



SPI I/F

USB

USB

SATA

SATA

AZALIA

AZALIA

5	4	3	2	1
D				
C				
B				
A				

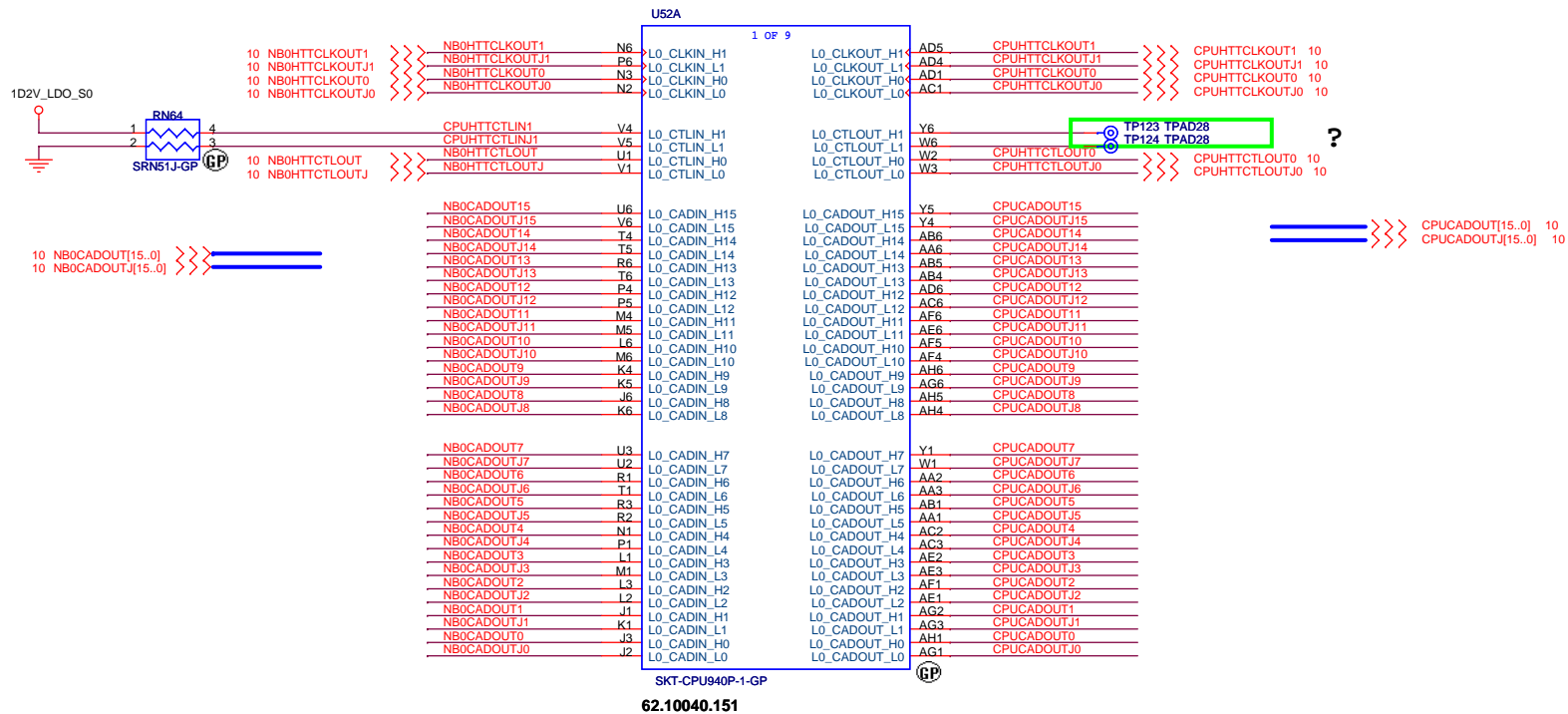
<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHANGE HISTORY		
Size	Document Number	Rev
A3	Yukon	SA
Date:	Thursday, July 03, 2008	Sheet 2 of 43



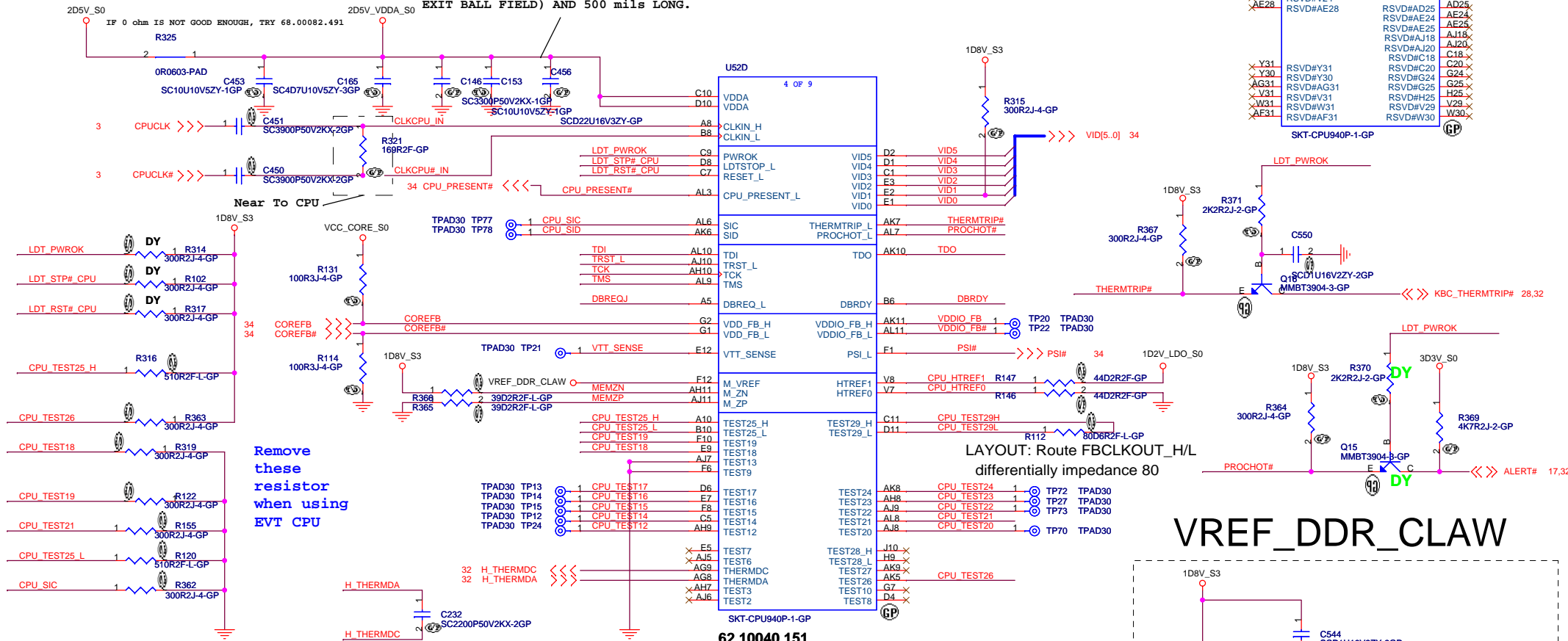


<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>CPU(1/4)_HyperTransport I/F</b>			
Size	Document Number	Rev	
A3		SA	
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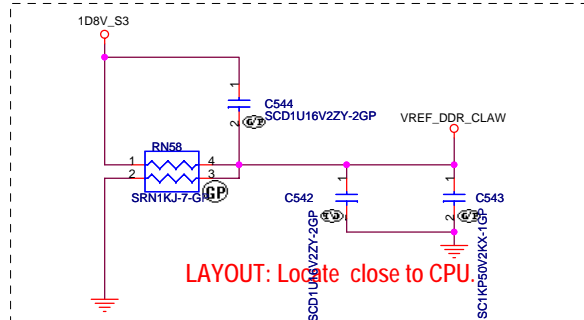
LYAOUT:ROUTE VDDA TRACE APPROX.  
50mils WIDE(USE 2X25 mil TRACES TO  
EXIT BALL FIELD) AND 500 mils LONG.



Remove  
these  
resistor  
when using  
EVT CPU

LAYOUT: Route FBCLKOUT\_H/L  
differentially impedance 80

VREF\_DDR\_CLAW



LAYOUT: Locate close to CPU

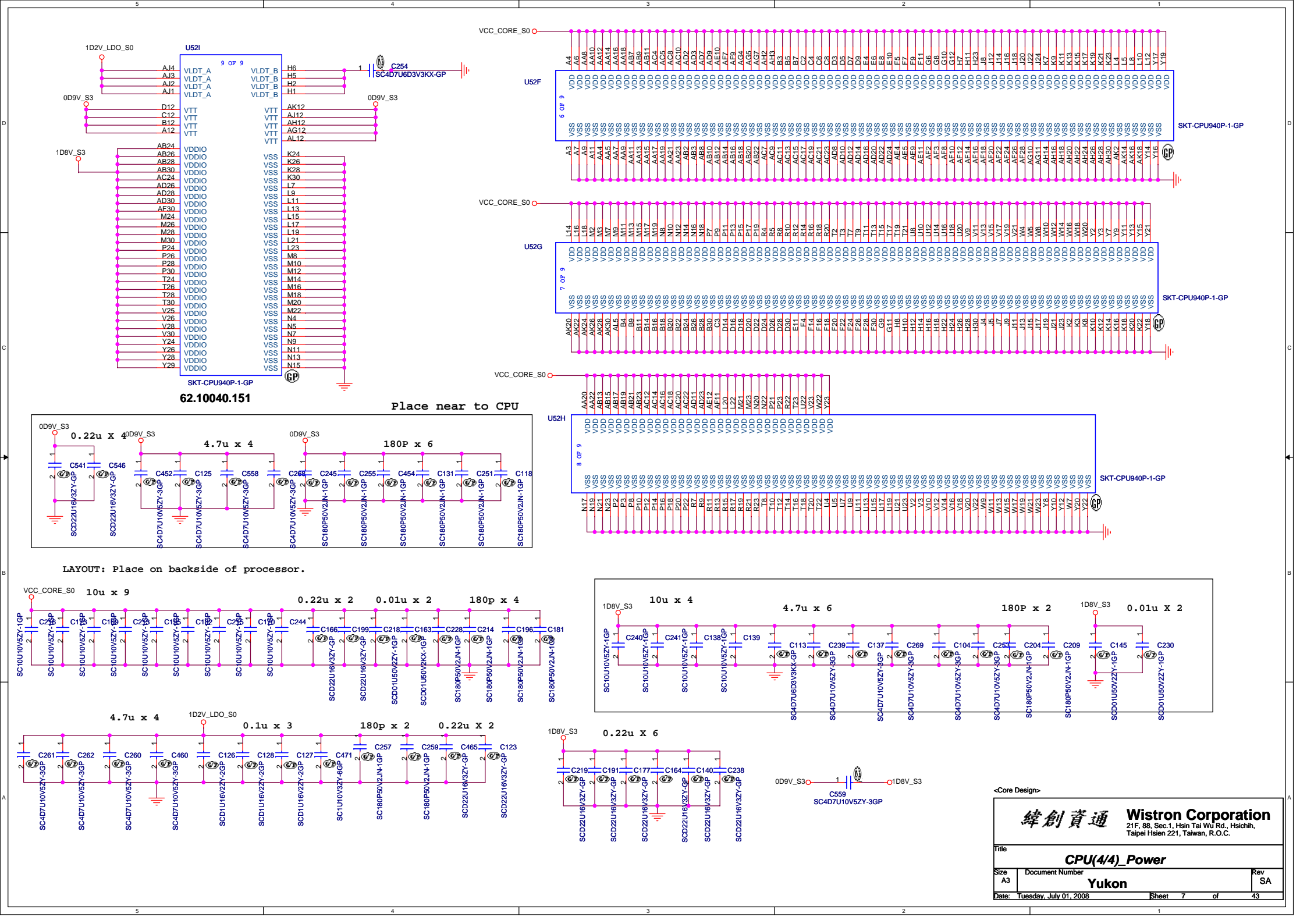
HDT Connectors

WWW.AliSaler.Com

<Core Design>

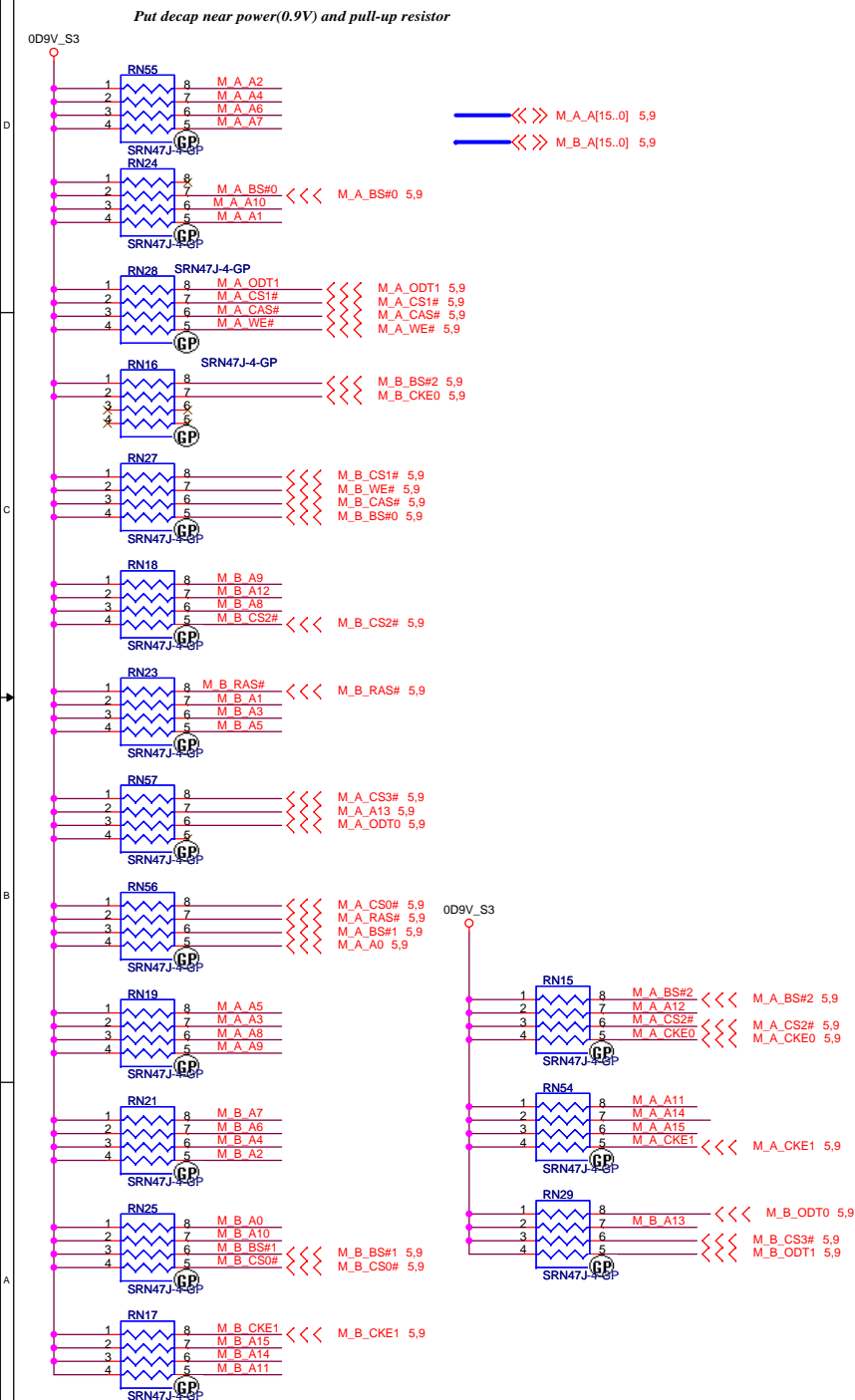
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>CPU(3/4)_Control &amp; Debug</b>		
Size	Document Number	Rev
A3		SA
Date: Thursday, July 03, 2008		
Sheet 6 of 43		

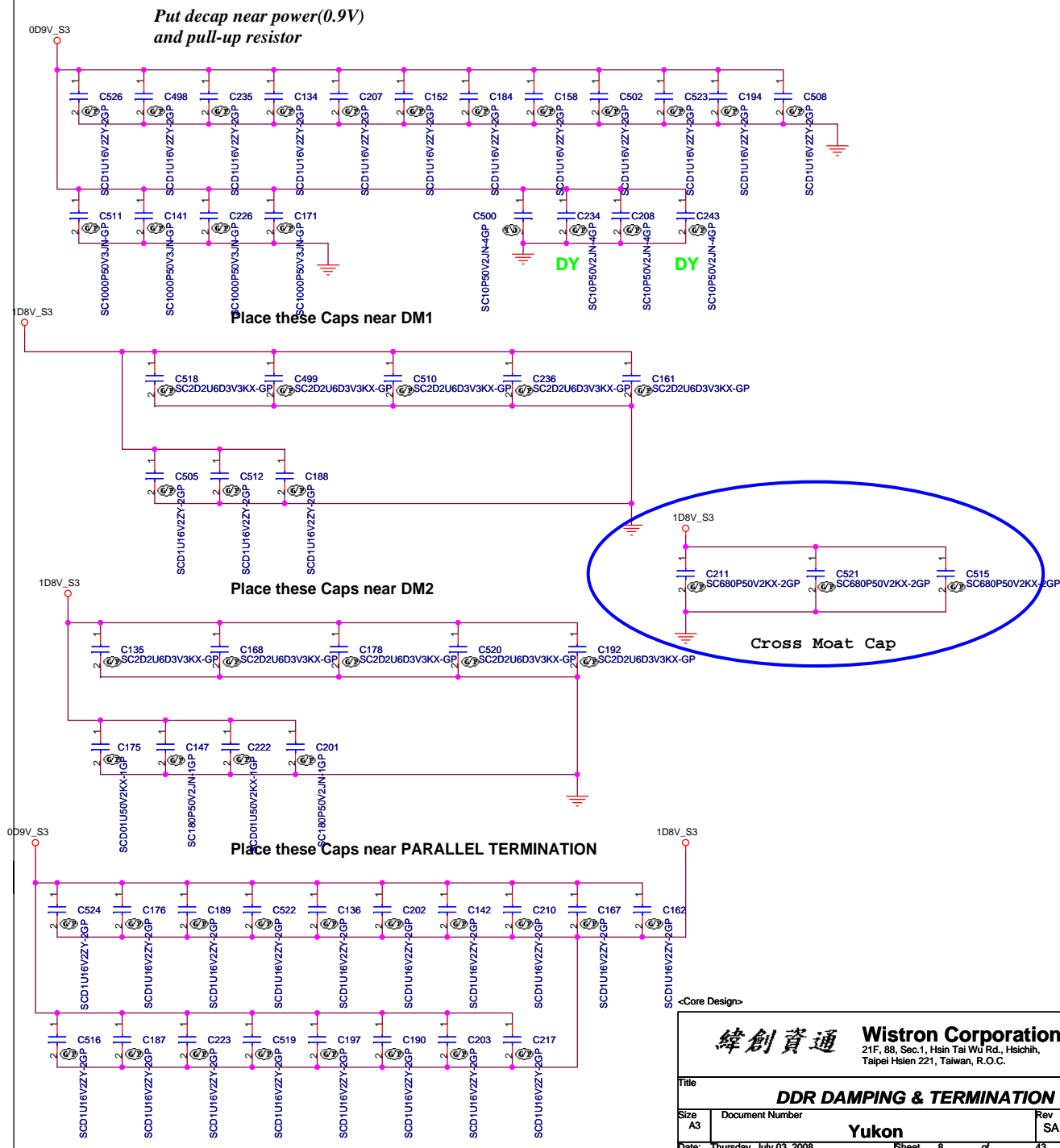




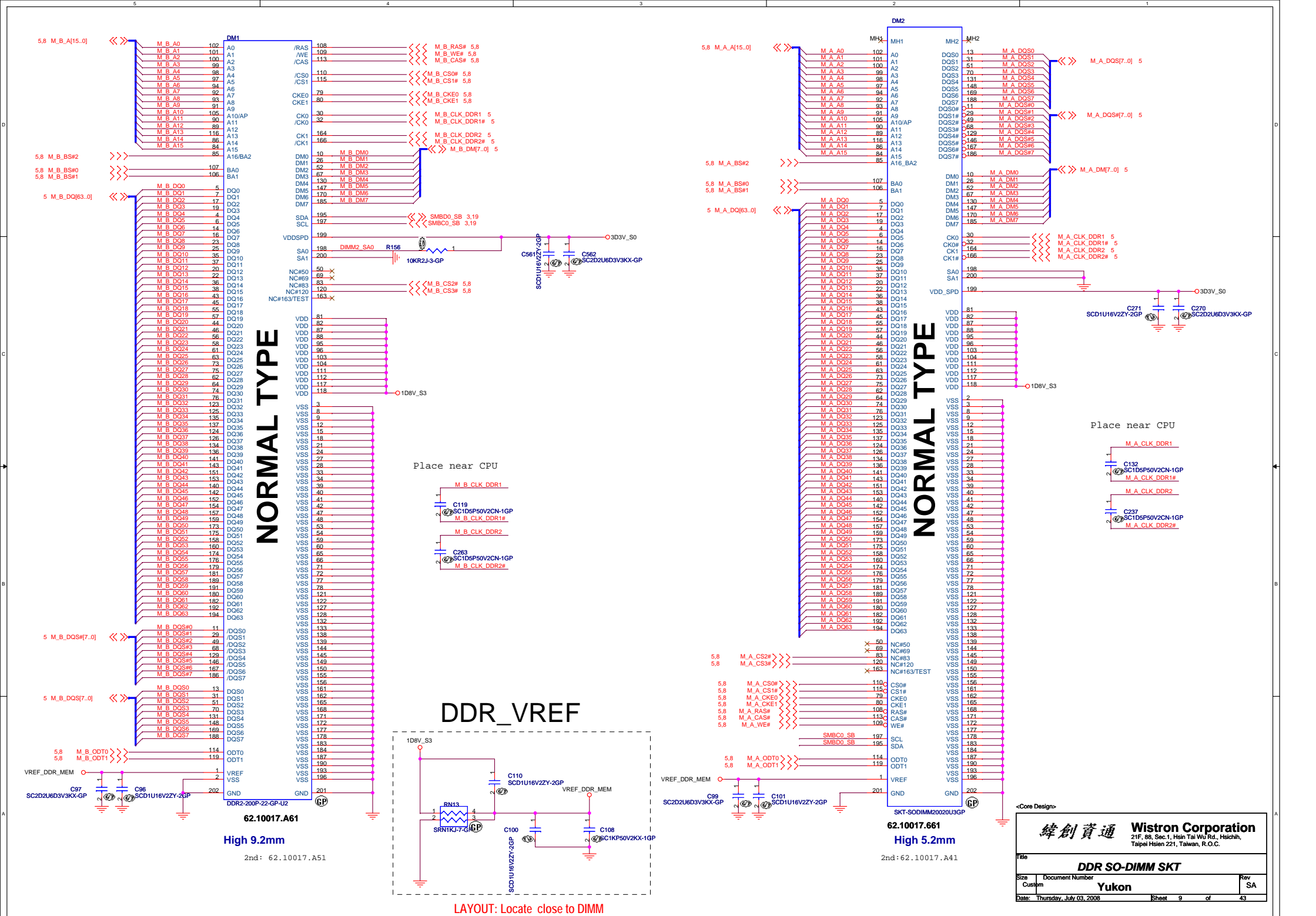
# PARALLEL TERMINATION



# Decoupling Capacitor

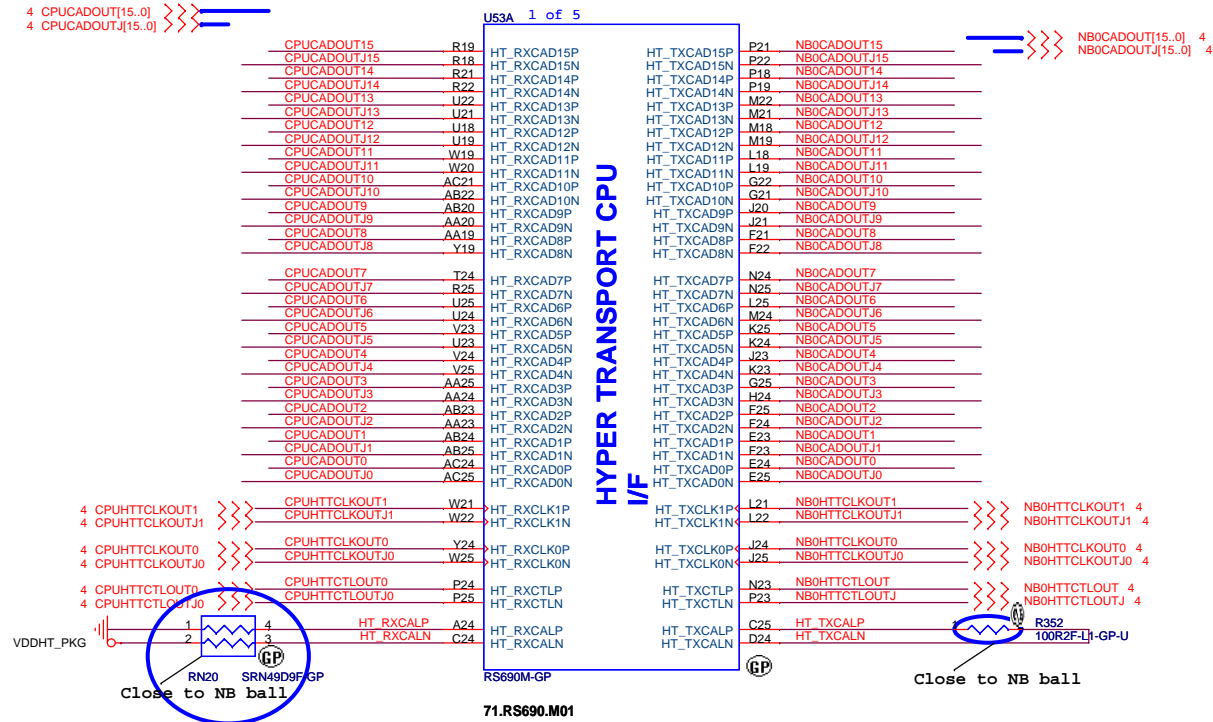






# CLAW HAMMER TO NB

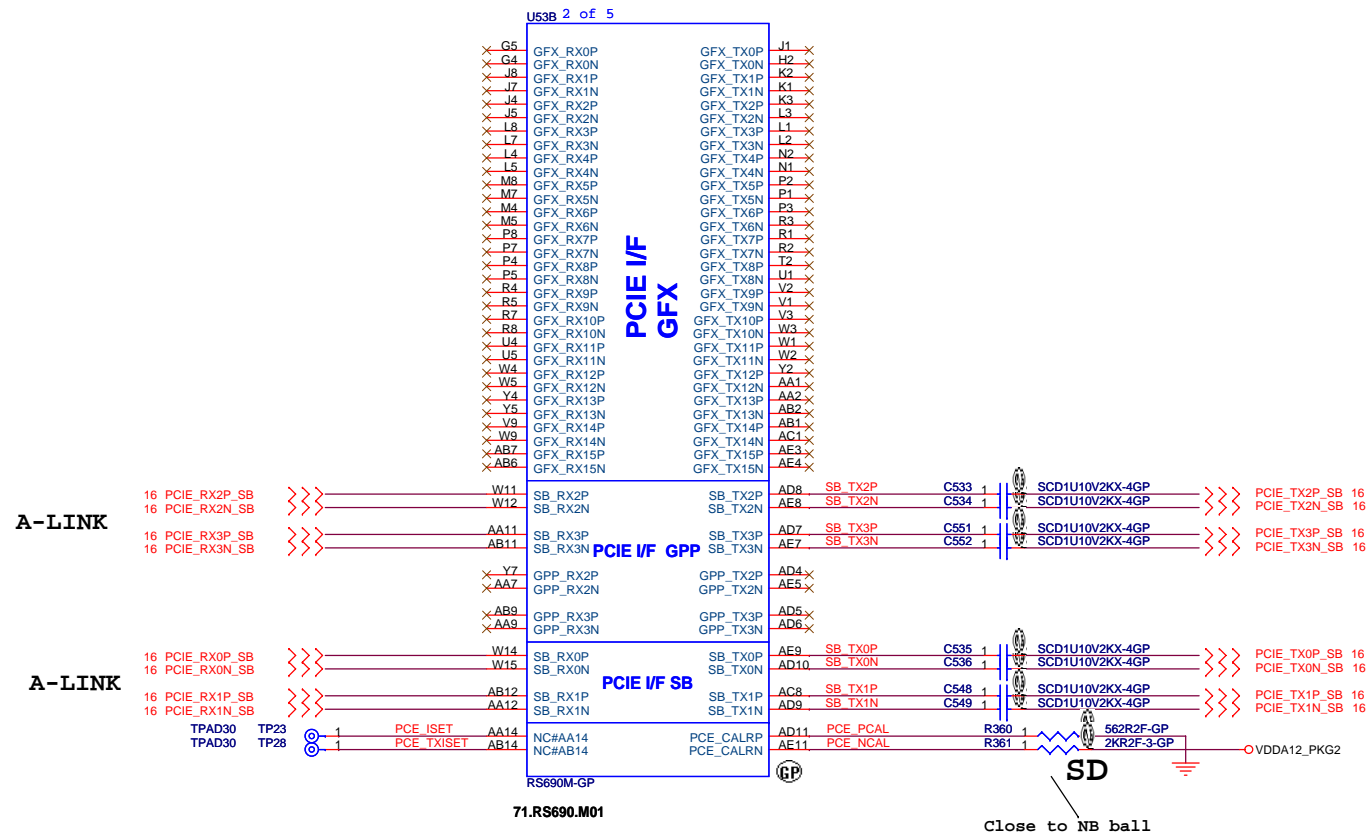
# NB TO CLAW HAMMER



<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			NB-RS690M HT	
Size	Document Number	Yukon		Rev
A3				SA
Date:	Thursday, July 03, 2008	Sheet	10 of 43	



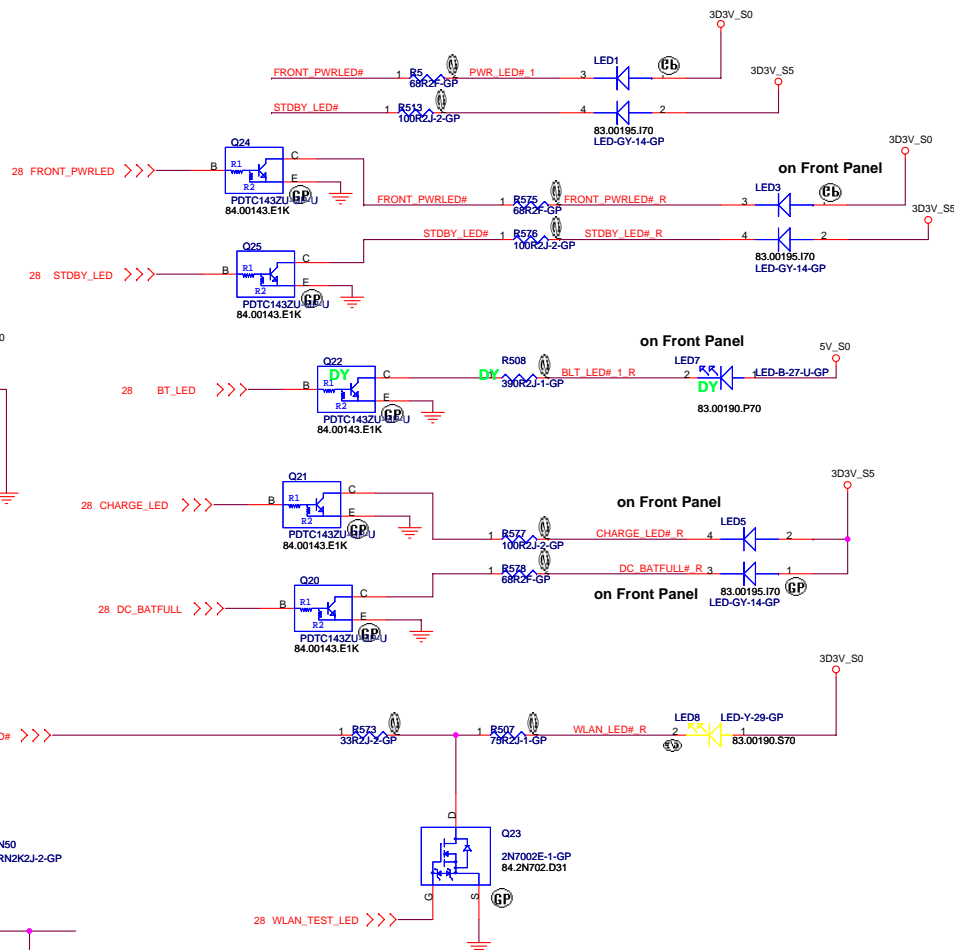
**A-LINK**  
**CLOSE TO NB**

<Core Design>

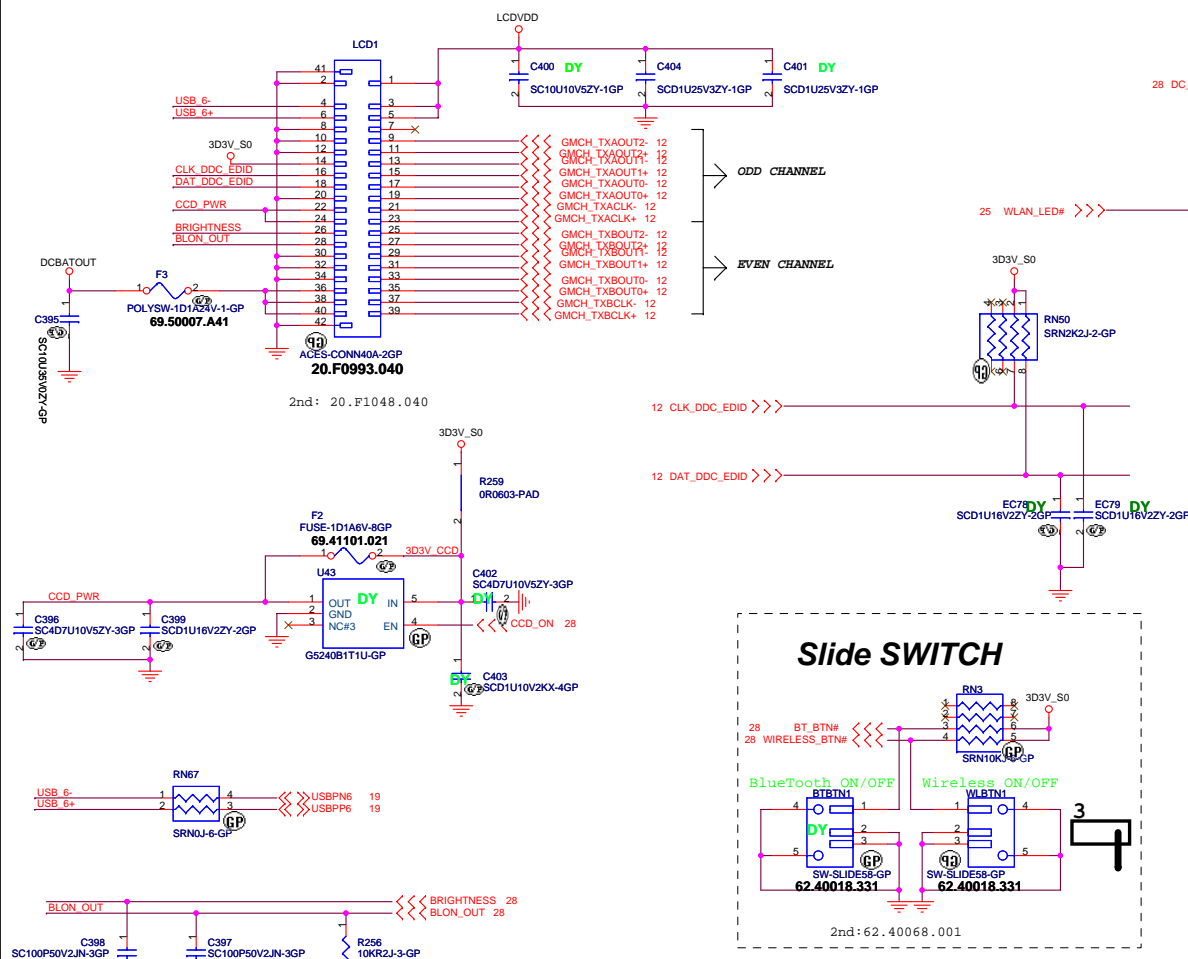
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NB-RS690M_MEM/PCIE_LINK I/F			
Size	Document Number		Rev
A3	Yukon		SA
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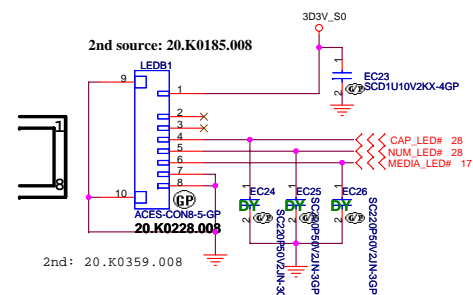




## LCD/INVERTER CONN



**LED BD**



<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih.

Title
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**LCD CONN & LED**

Size

Document Number

00 00

Rev

Date: Thursday, July 03, 2008

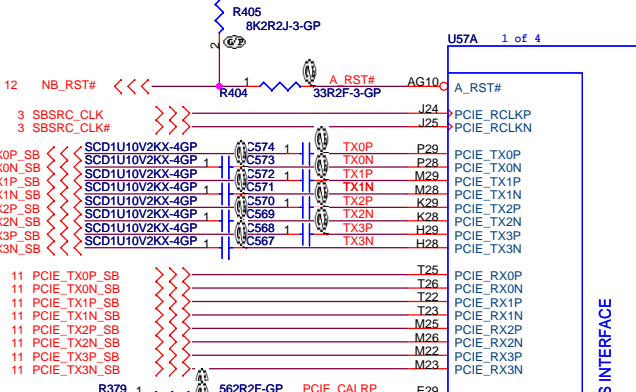
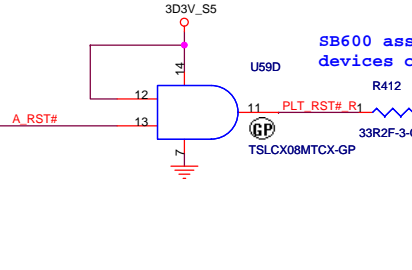
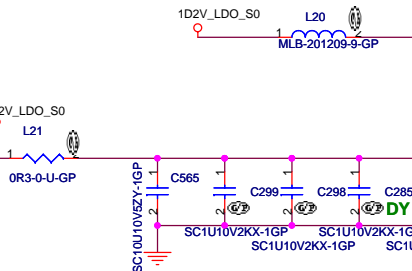
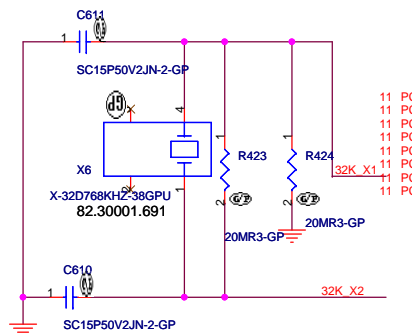
Sheet 14 of 4

43

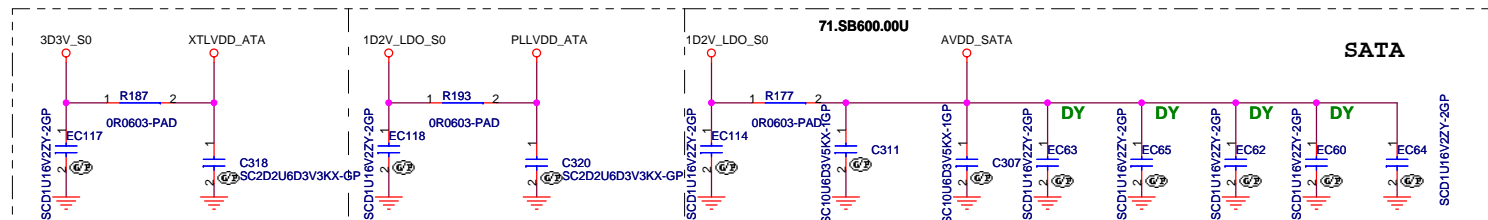
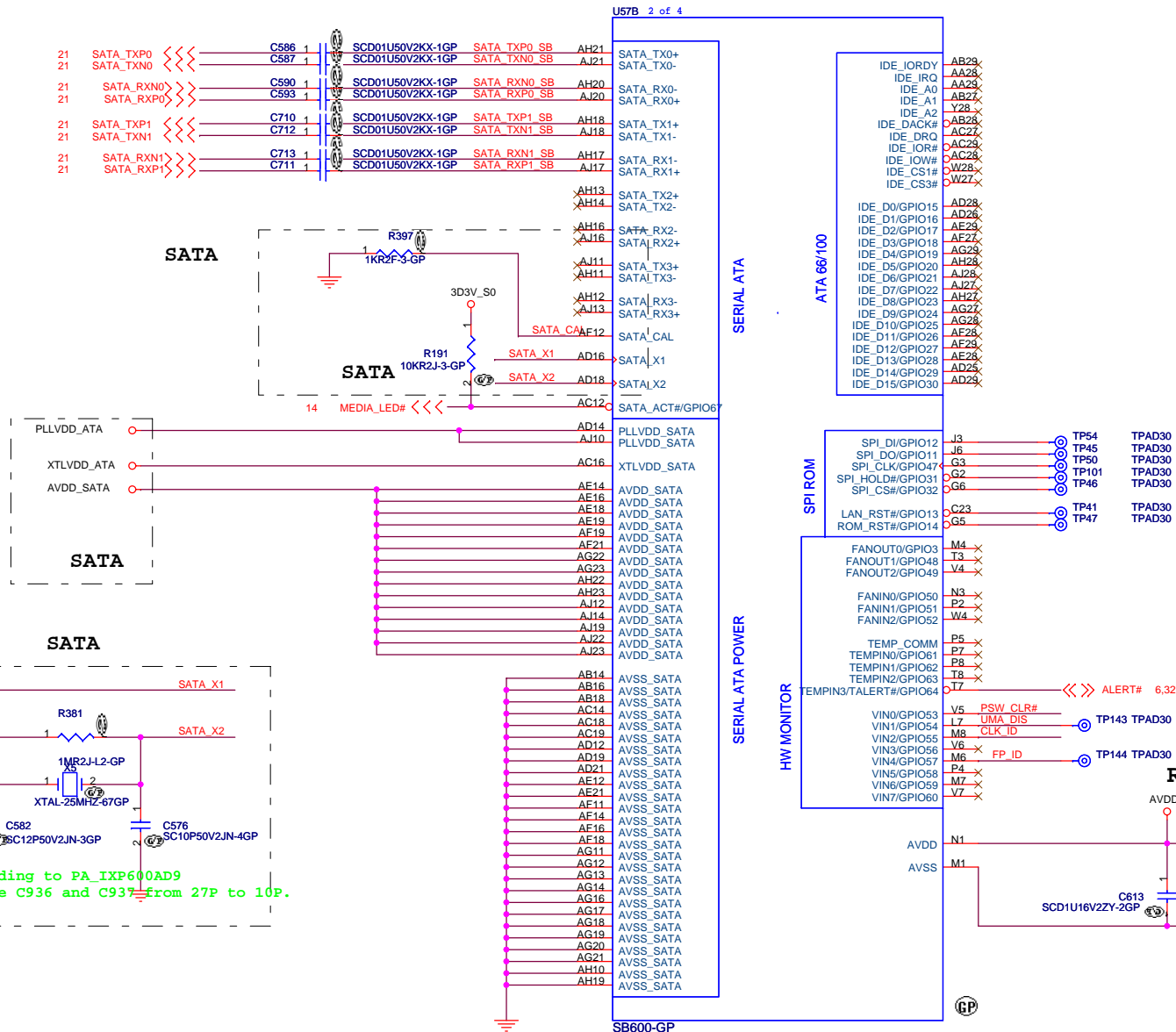




Place these components close to U13 and use ground guard for 32K\_X1 and 32K\_X2.



PLACE SATA AC DECOUPLING  
CAPS CLOSE TO SB460

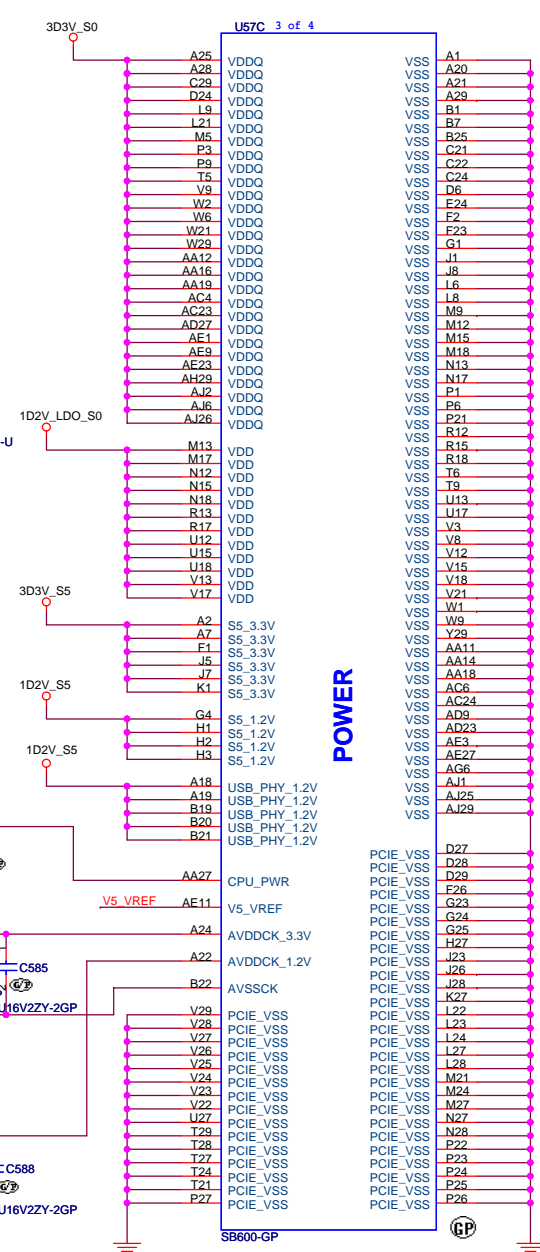


**<Core Design>**

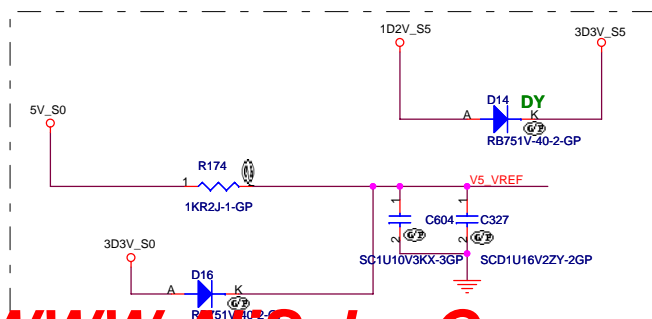
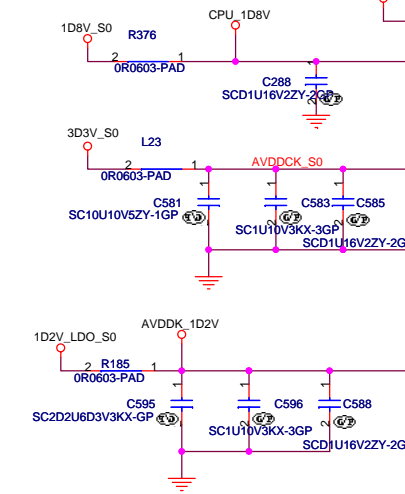
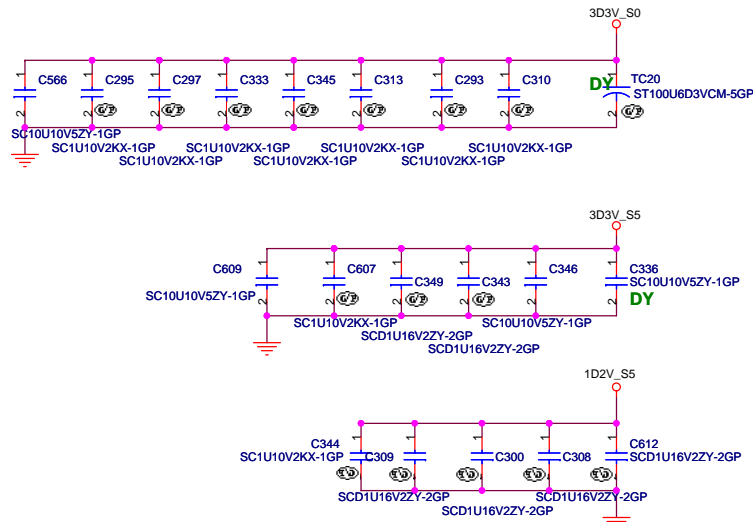
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

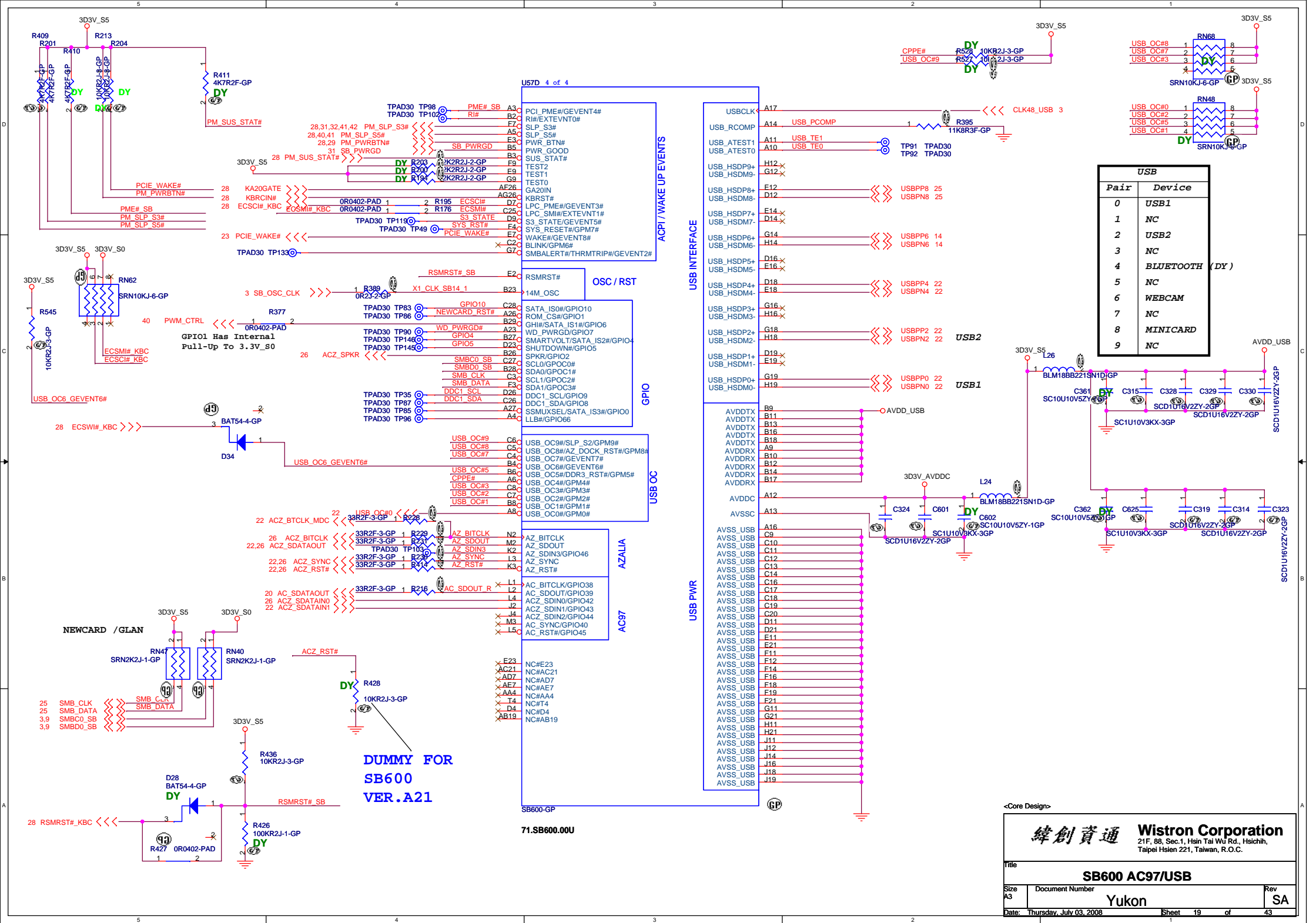
Title	SB600 ACPI/GPIO/SATA/IDE (2 of 5)
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Size A3	Document Number <b>Yukon</b>	Rev <b>SA</b>
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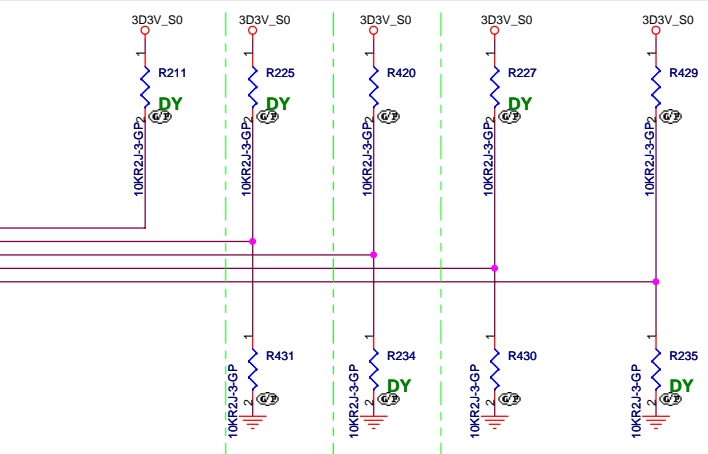
Place near to SB600





PCI\_CLK4  
PCI\_CLK6  
PCI\_CLK0  
PCI\_CLK1

19 AC\_SDATAOUT  
16,28 PCLK\_KBC  
15 CLK33\_LPCROM  
16,28 PCI\_CLK0  
16 PCLK\_PCM

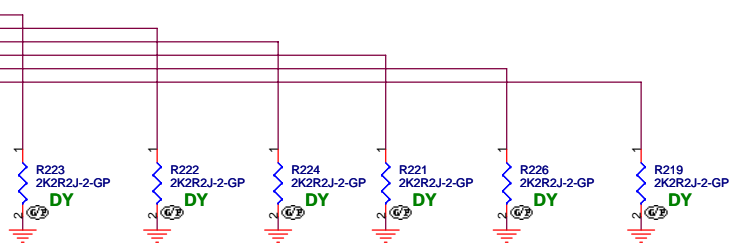


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[23..28]

16 PCI\_AD28  
16 PCI\_AD27  
16 PCI\_AD26  
16 PCI\_AD25  
16 PCI\_AD24  
16 PCI\_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通

Wistron Corporation

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Title

SB600 STRAPPING PIN

Size A3

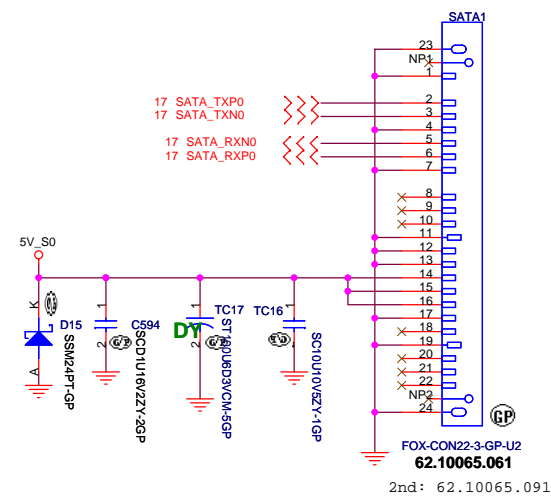
Document Number

Rev SA

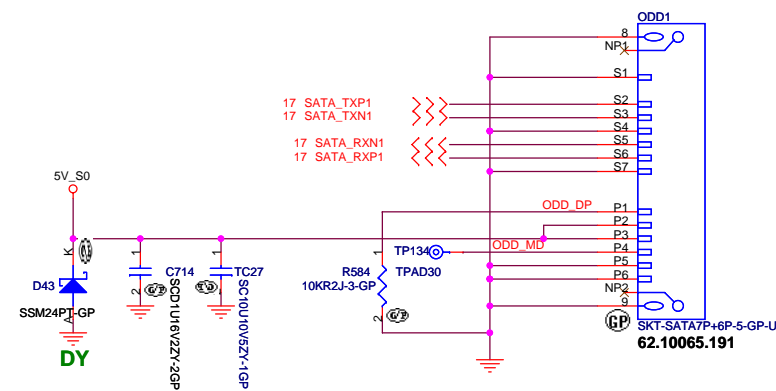
Date: Thursday, July 03, 2008

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SATA HD Connector



SATA ODD Connector

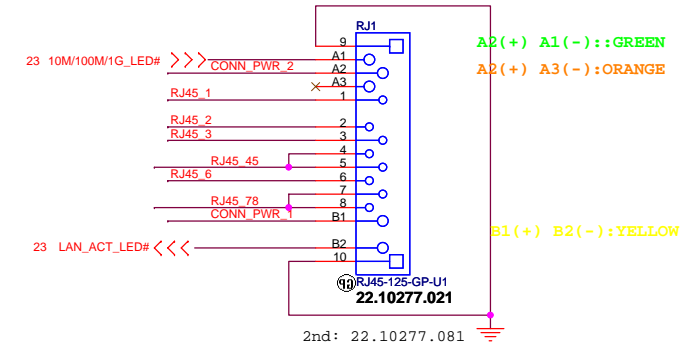
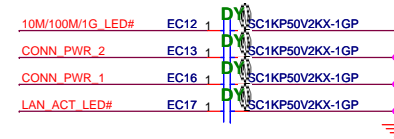




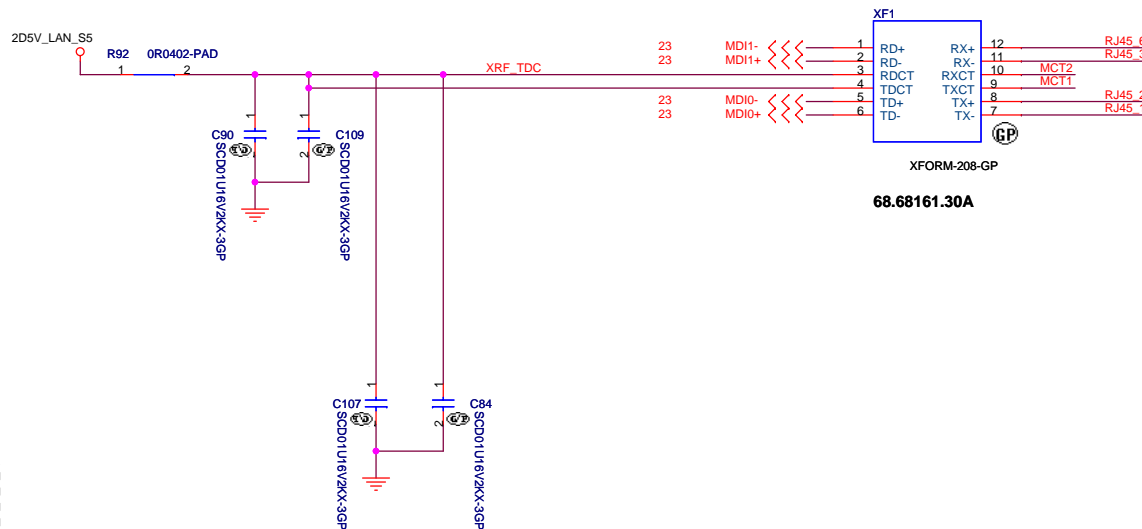




## LAN Connector



## 10/100 Lan Transformer

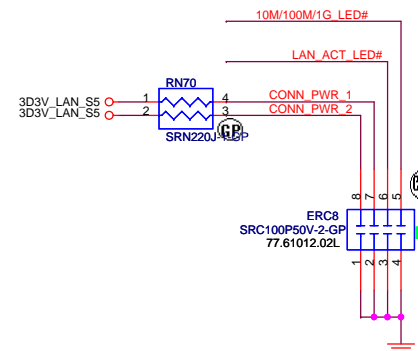
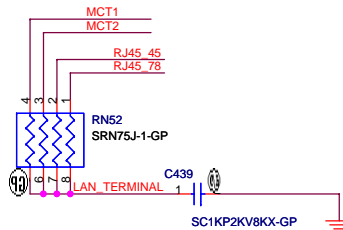


1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

10/100 LAn Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
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## LAN Connector

Size

Document Number

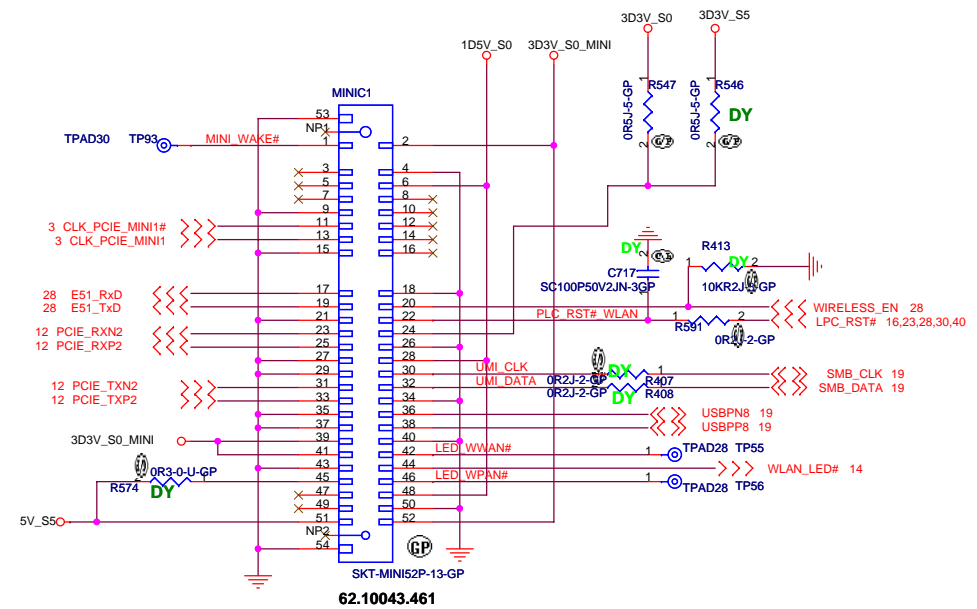
## Yukon

Date: Thursday, July 03, 2008

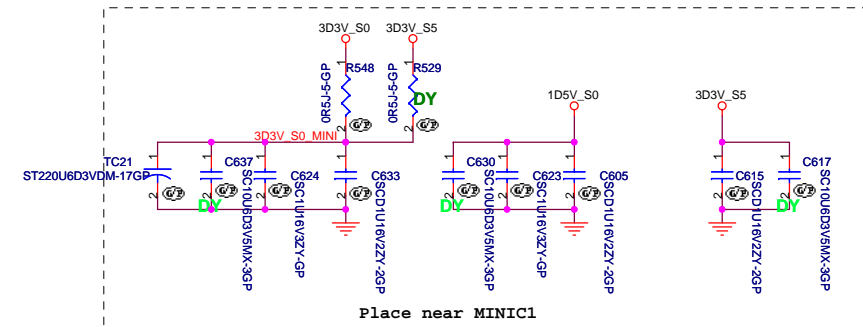
Sheet 24 of

Rev

### *Mini Card Connector*



2nd: 20.F1049.052



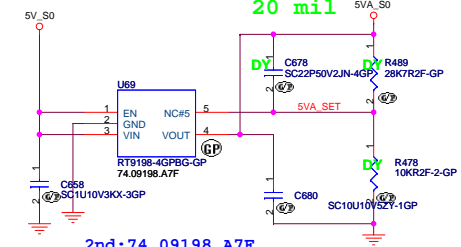
**bom1**

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>MINI CARD / NEW CARD</b>			
Size	Document Number		Rev
	<b>Yukon</b>		SA
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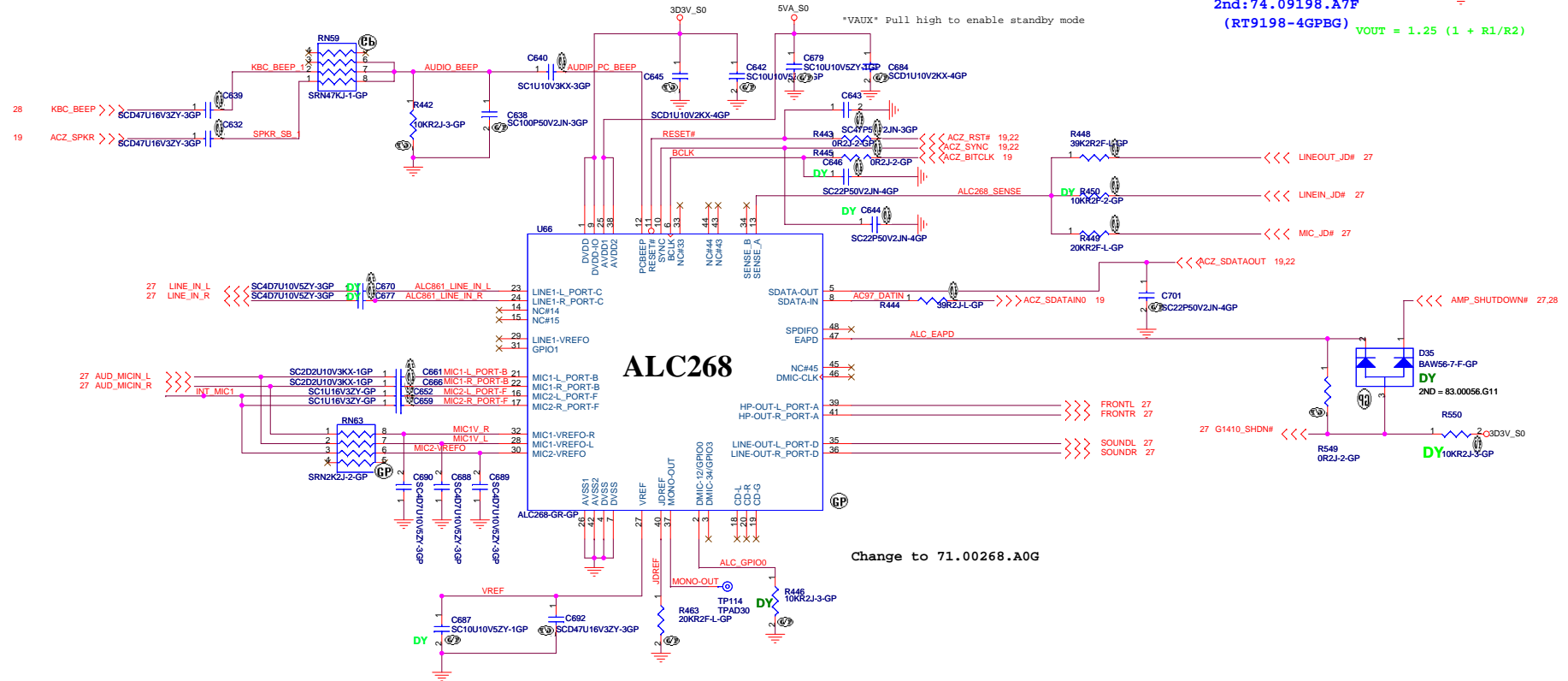
## POWER GENERATE

\*Layout\*  
20 mil 5VA



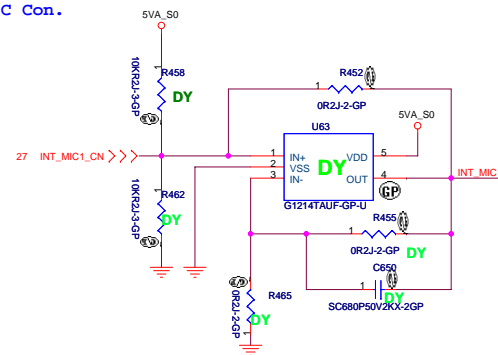
2nd:74.09198.A7F  
(RT9198-4GPBG)

G)  $V_{OUT} = 1.25 (1 + R1/R2)$



Change to 71.00268.A0G

Near INTMIC Con.



<Variant Name:

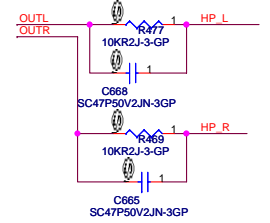
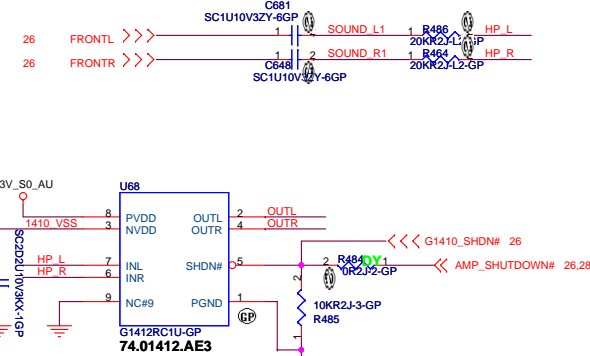
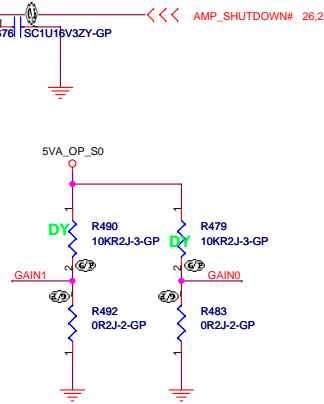
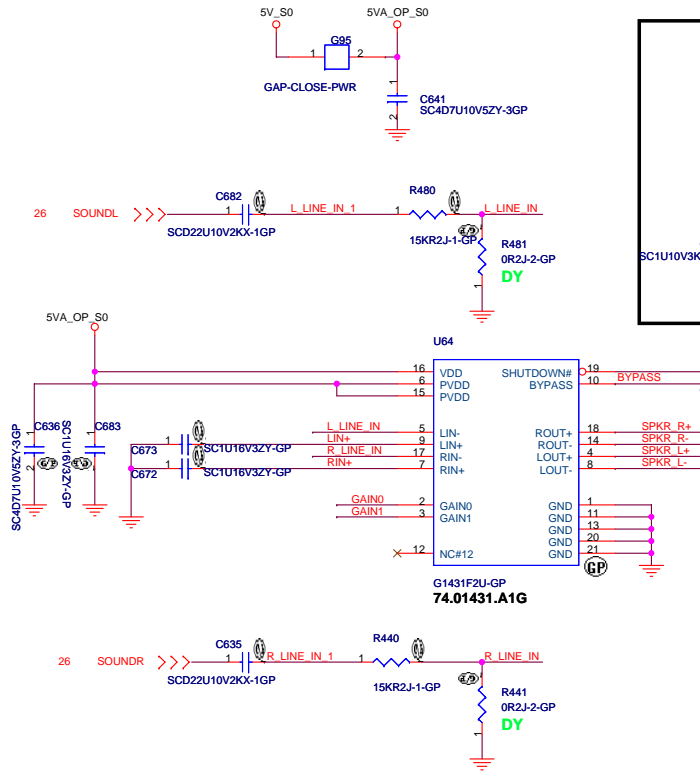
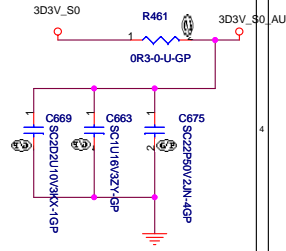
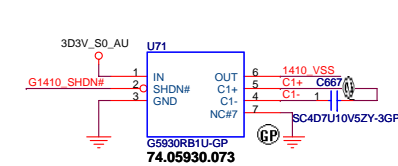
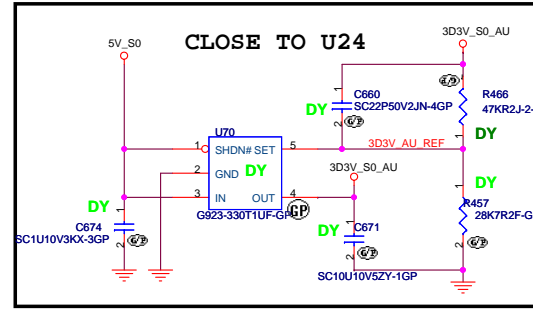
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>AZALIA CODEC - ALC268</b>
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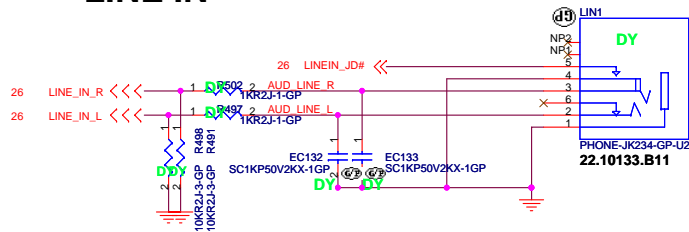
Size	Document Number	Yukon	Rev
			SA

# AUDIO OP AMPLIFIER

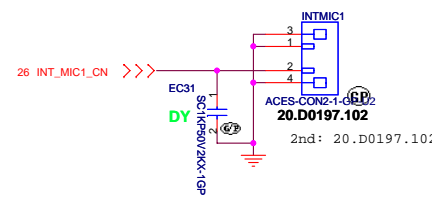
KBC\_MUTE\_GPIO8



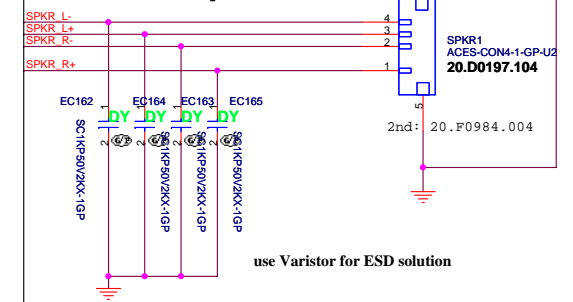
## LINE IN



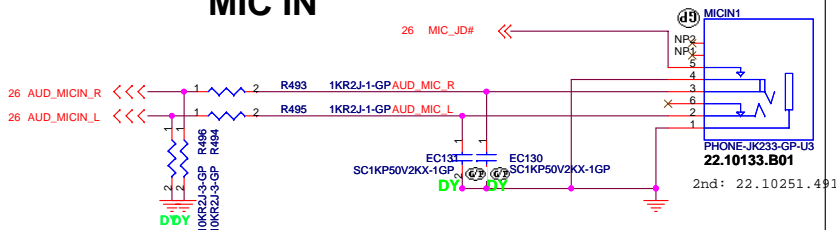
## Internal Microphone



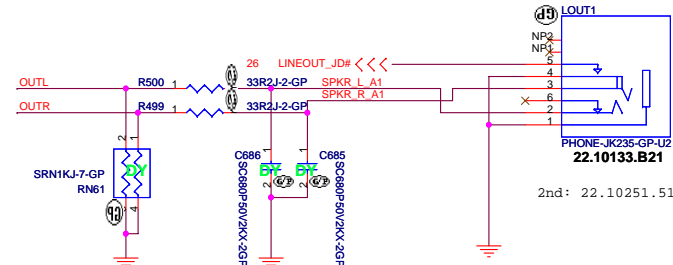
## Internal Speaker



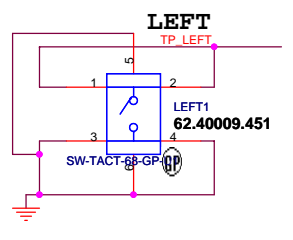
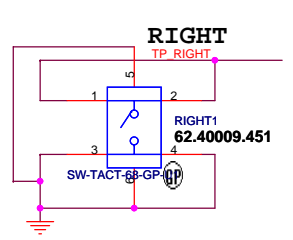
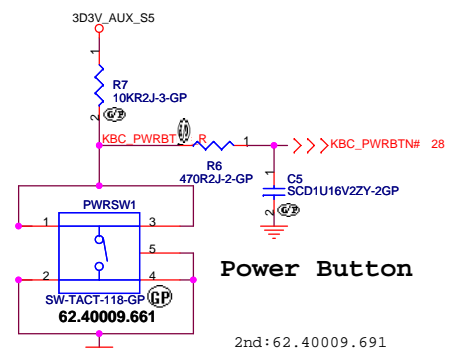
## MIC IN



## LINE OUT

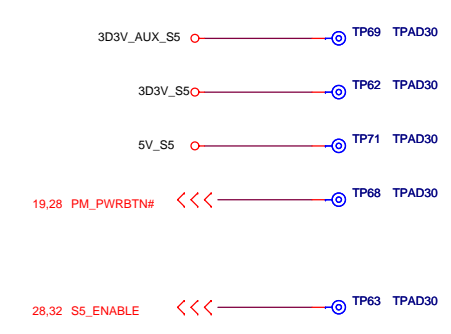
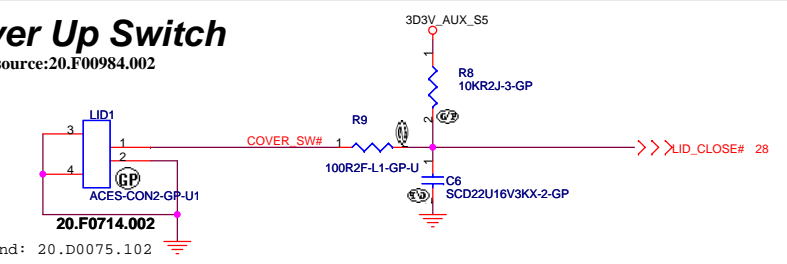




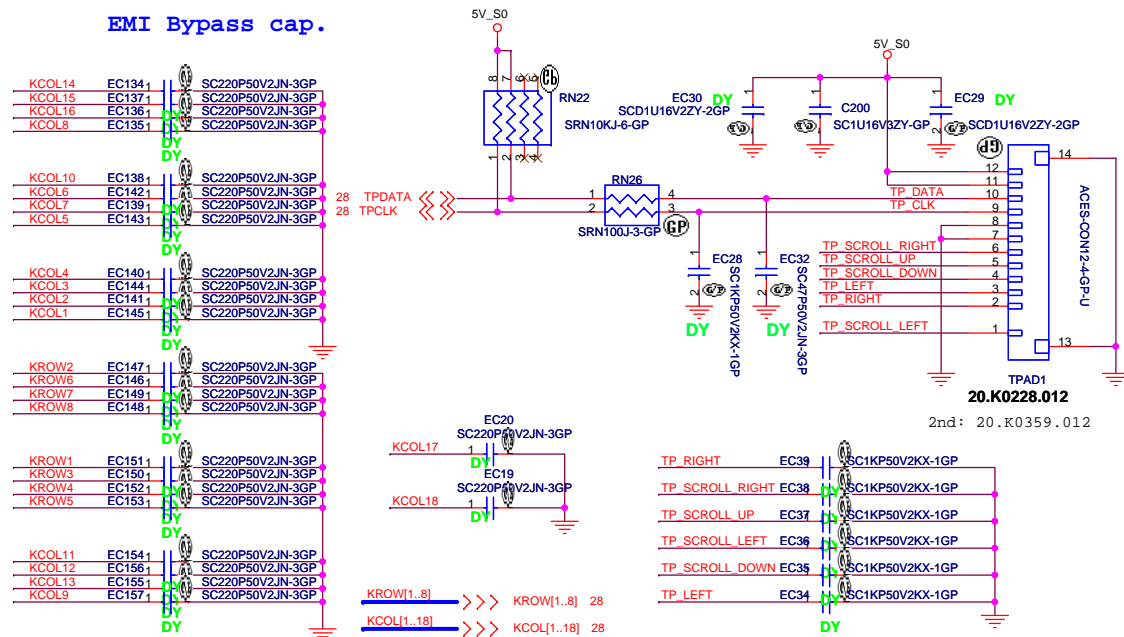
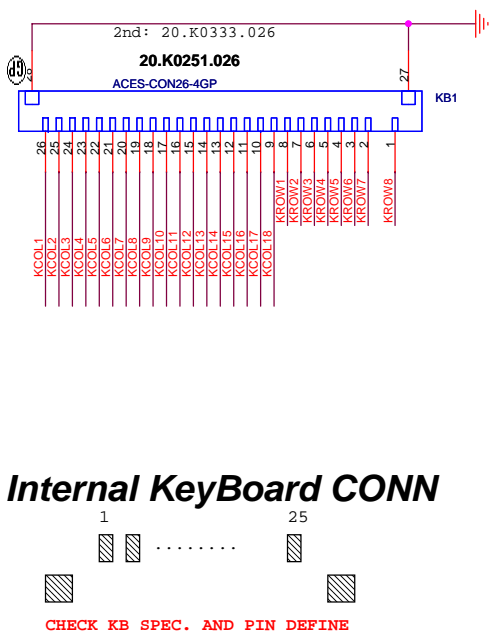


## Cover Up Switch

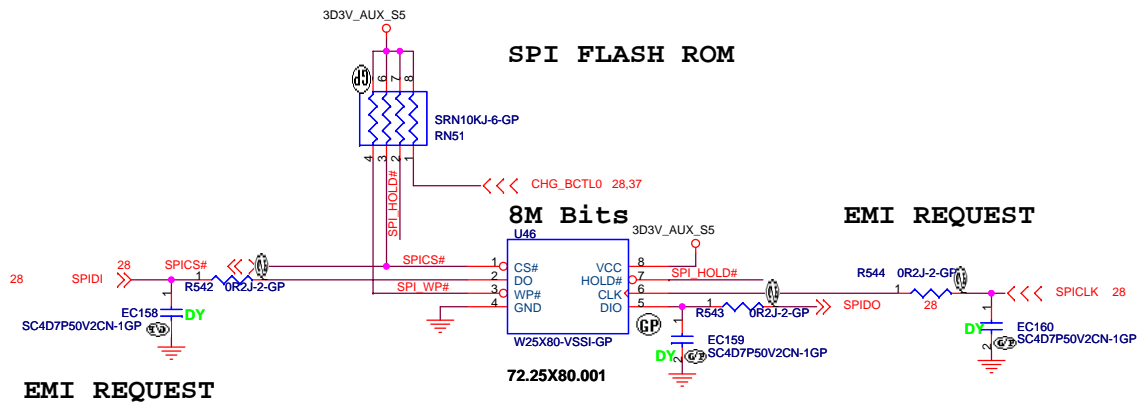
2nd source: 20.F00984.002



Test Point 放在 Dimm Door 打開可量測處

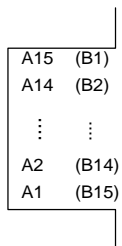






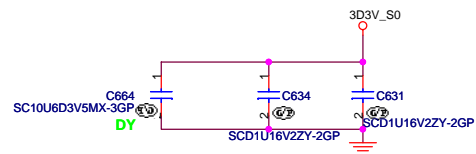
EMI REQUEST

TOP VIEW

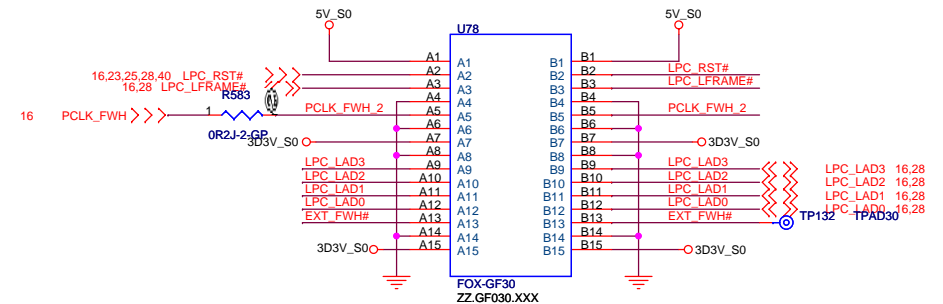


(BOTTOM VIEW)

Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46

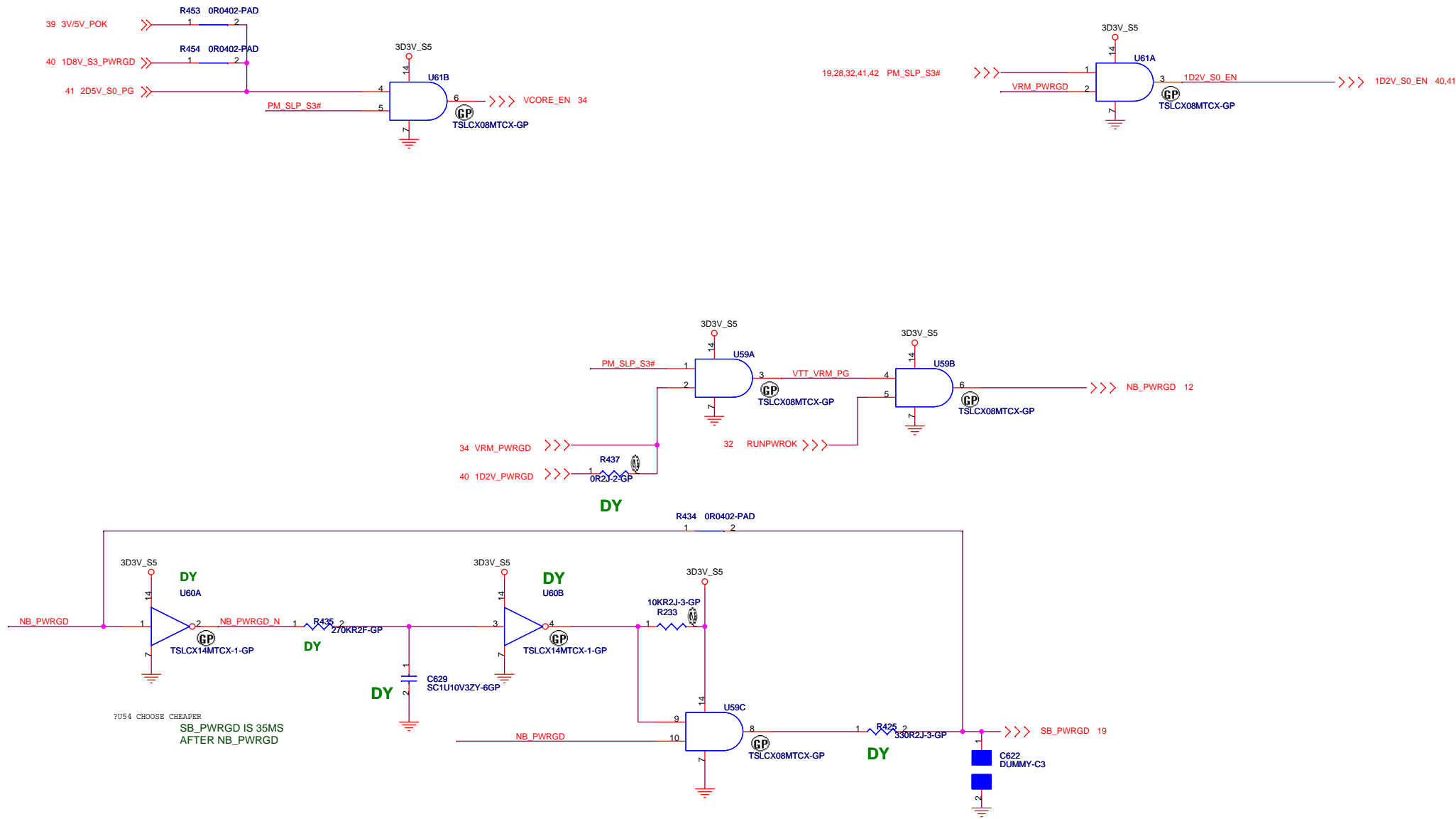


GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

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Title	
BIOS	
Size A3	Document Number Yukon
Date: Thursday, July 03, 2008	Rev SA
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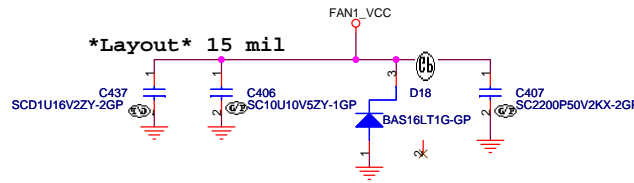
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>POWERGOOD&amp;ENABLES(1/2)</b>			
Size A3	Document Number <b>Yukon</b>	Rev SA	
Date: Thursday, Jul 03, 2008		Sheet 31 of 43	

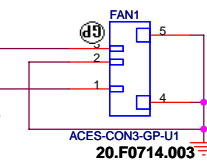
Setting T8 as 90 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

\*Layout\* 15 mil

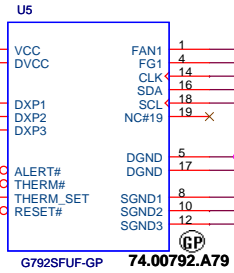
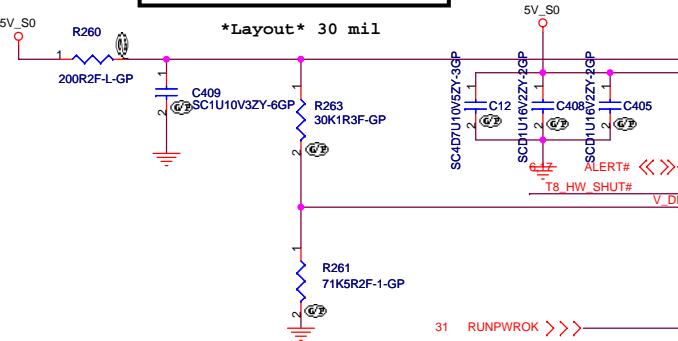


\*Layout\* 15 mil



2nd: 20.D0246.103

\*Layout\* 30 mil



DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

Place near chip as close as possible

2.System Sensor,  
Put between CPU and NB.

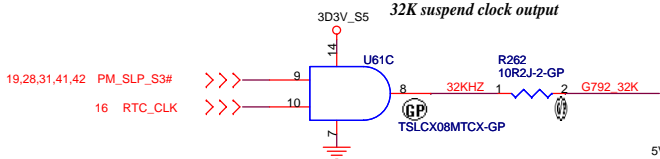
3.T8 Sensor

>>> H\_THERMDA 6

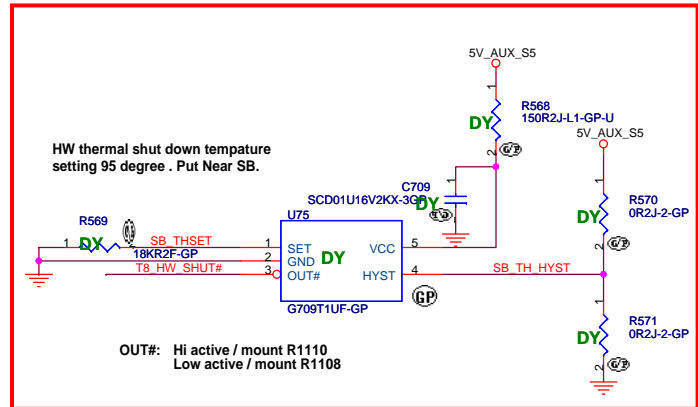
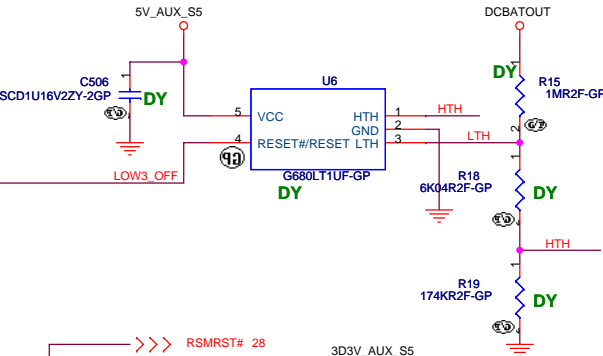
<<< H\_THERMDC 6

1.For CPU Sensor

32K suspend clock output



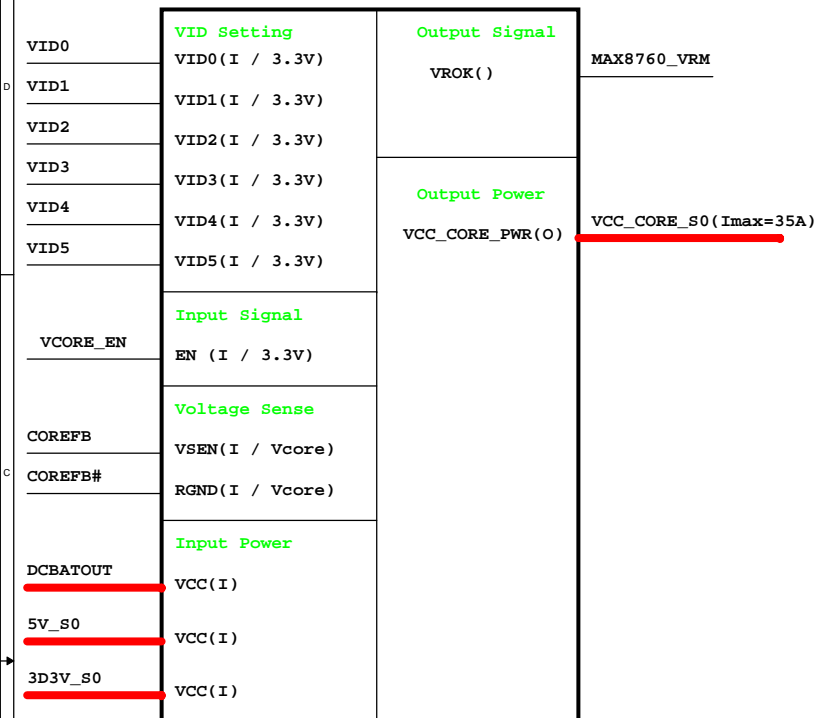
HW Thermal Throttling BL3#



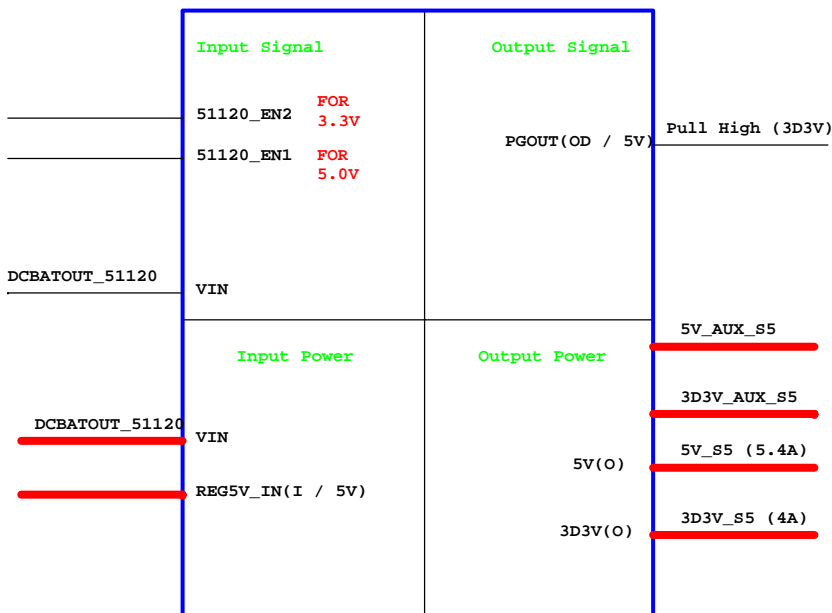
OUT#: Hi active / mount R1110  
Low active / mount R1108

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Size A3	Document Number Yukon	Rev SA	
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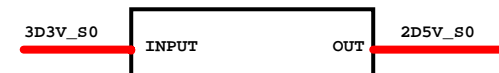
CPU\_CORE  
ISL6264CRZ



TI TPS51120  
3D3V/5V



2D5V\_S0



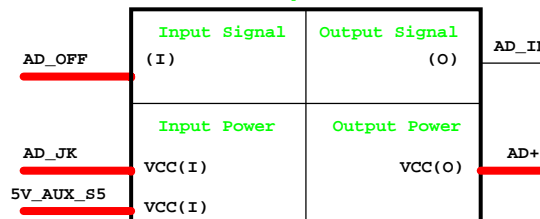
APL5913

1D8V\_S5

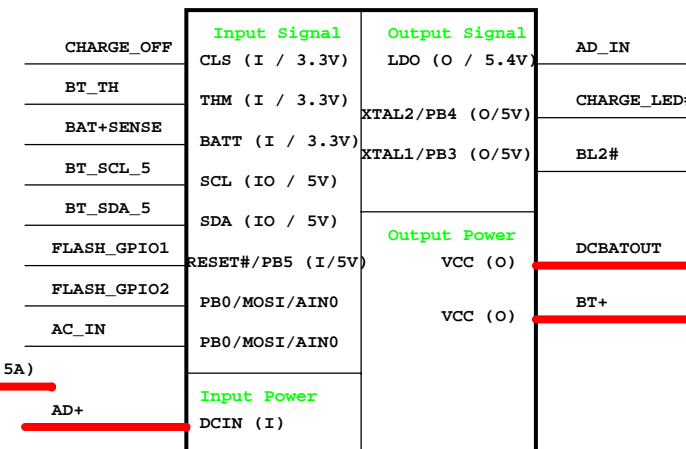


APL5332KAC-TRLGP

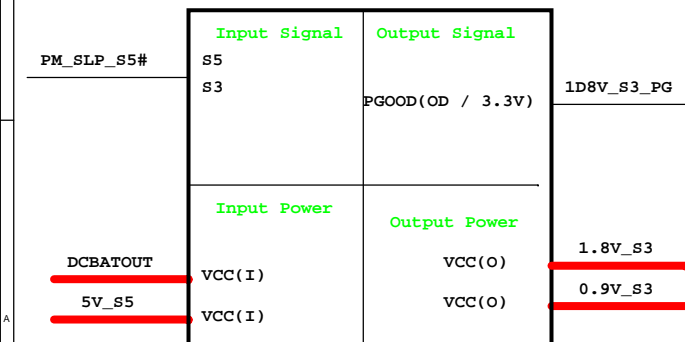
Adapter



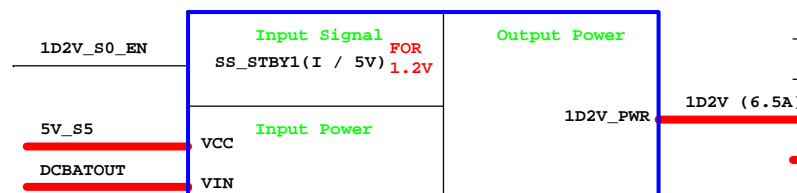
Charger\_ISL6255



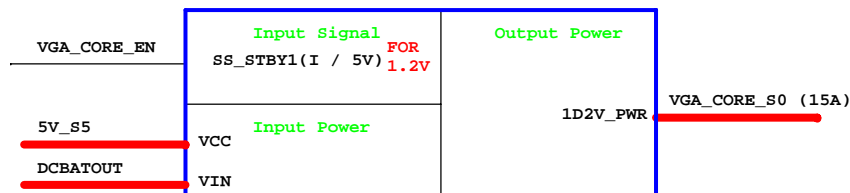
TI TPS51116  
1.8V / 0.9V



ISL6268\_1D2V



ISL6268\_VGA\_CORE

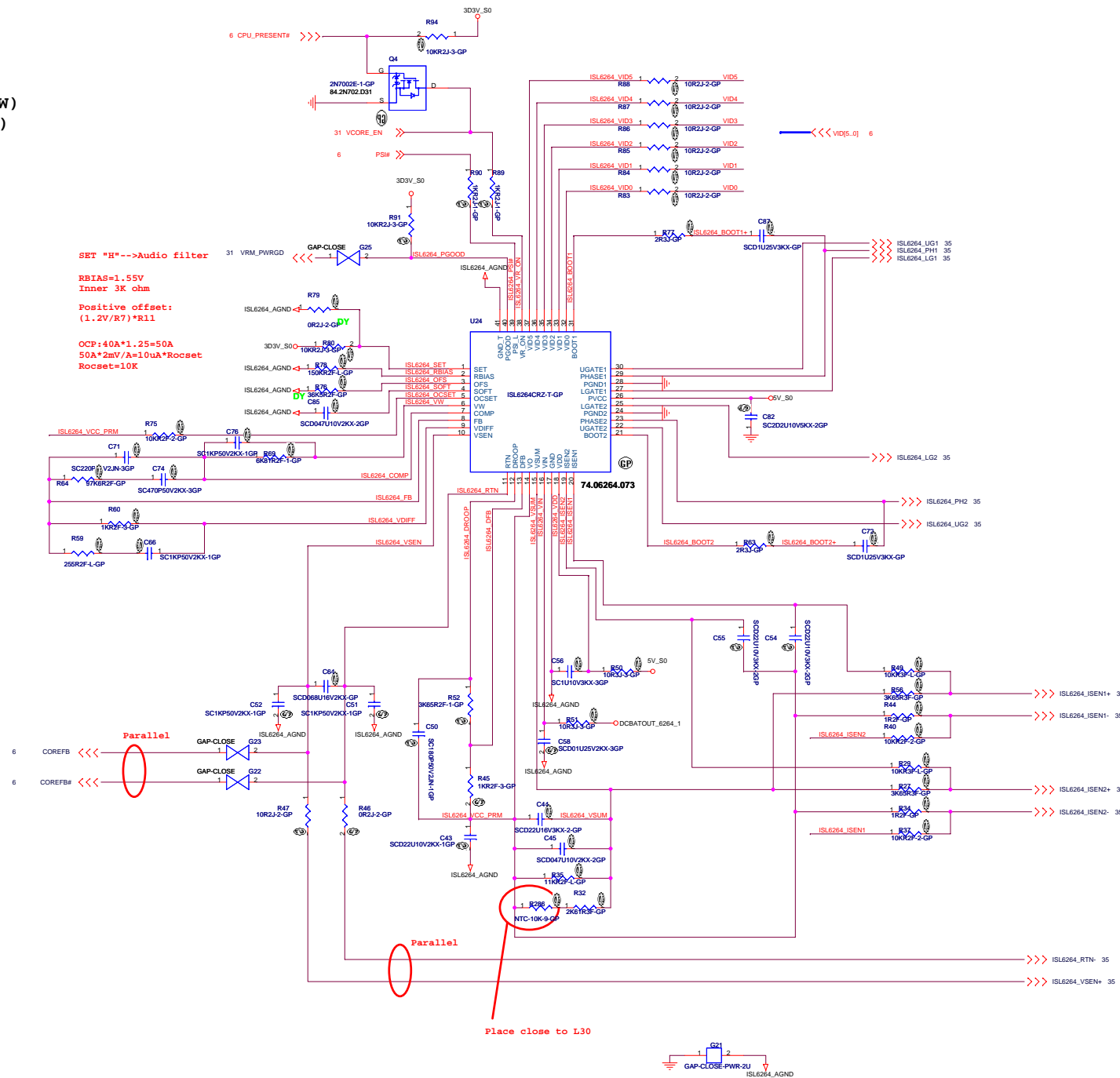


<Core Design>

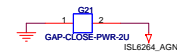
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Power Block Diagram		
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VID=1.20V(25W)/1.15V(35W)  
Iomax=21A(25W)/35A (35W)  
OCP=40A~45A

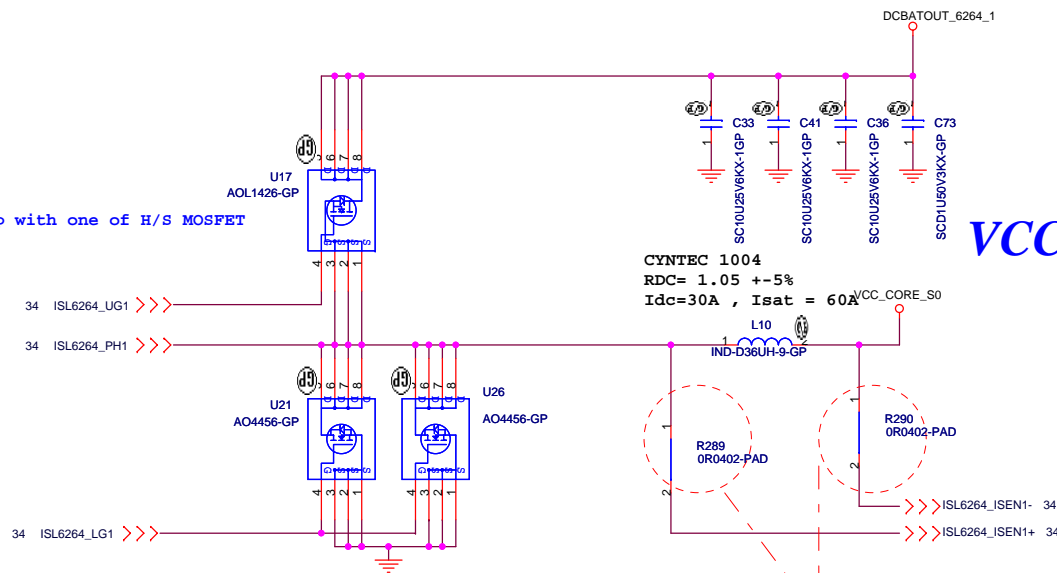
V1D5	V4D4	V1D3	V1D2	V1D1	V1D0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.505
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	1	0	0	0	1.375
0	0	1	0	0	1	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	1	0	0	0	0	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	1	0	0	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



Place close to L30



Overlap with one of H/S MOSFET



**VCC\_CORE\_S0**

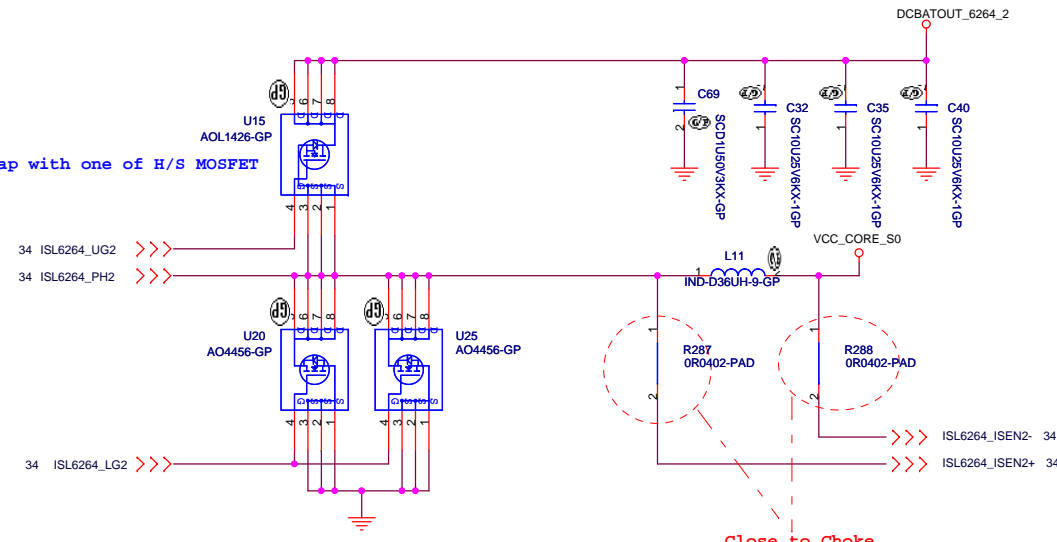
CYNTEC 1004

RDC= 1.05 +-5%

Idc=30A , Isat = 60A

Close to Choke

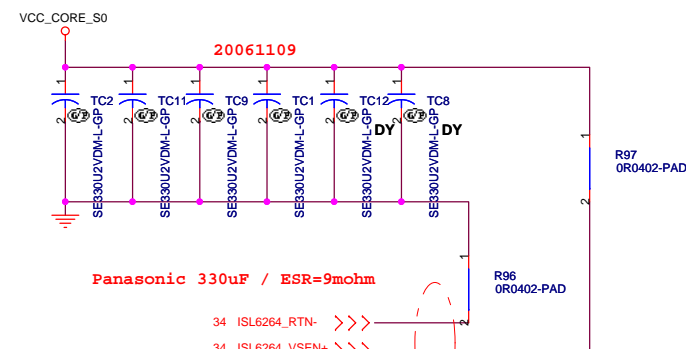
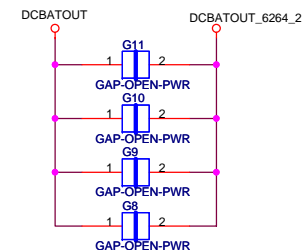
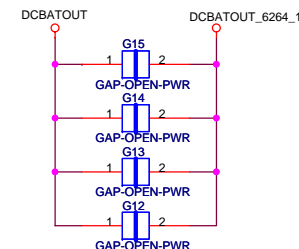
Overlap with one of H/S MOSFET



CYNTEC 1004

RDC= 1.05 +-5% , Idc=30A , Isat = 60A

Close to Choke



Panasonic 330uF / ESR=9mohm

Parallel

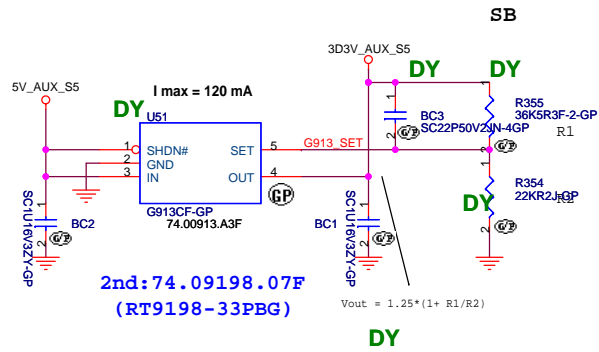
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU Vcore Power_2			
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# Aux Power

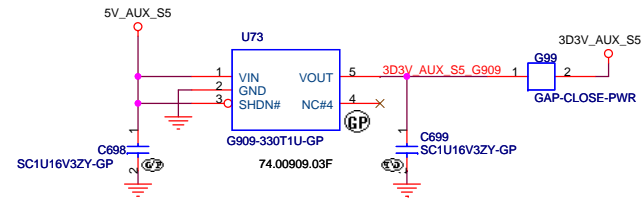
3D3V\_AUX\_S5



2nd: 74.09198.07F  
(RT9198-33PBG)

# Aux Power

3D3V\_AUX\_S5



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**3D3V AUX**

Size  
A3

Document Number

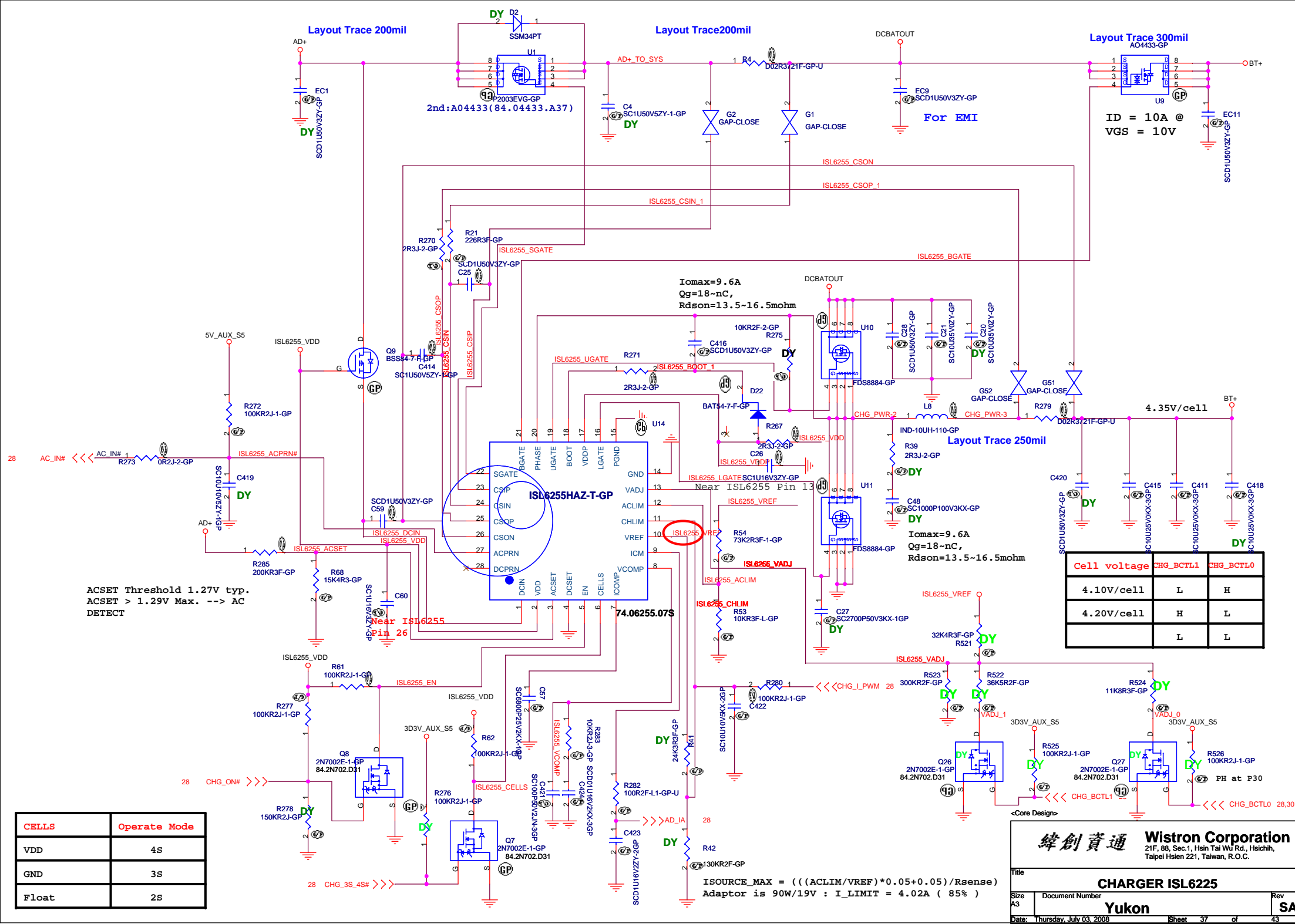
Yukon

Rev  
SA

Date: Tuesday, July 01, 2008

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A	B	C	D	E
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## BATTERY CONNECTOR

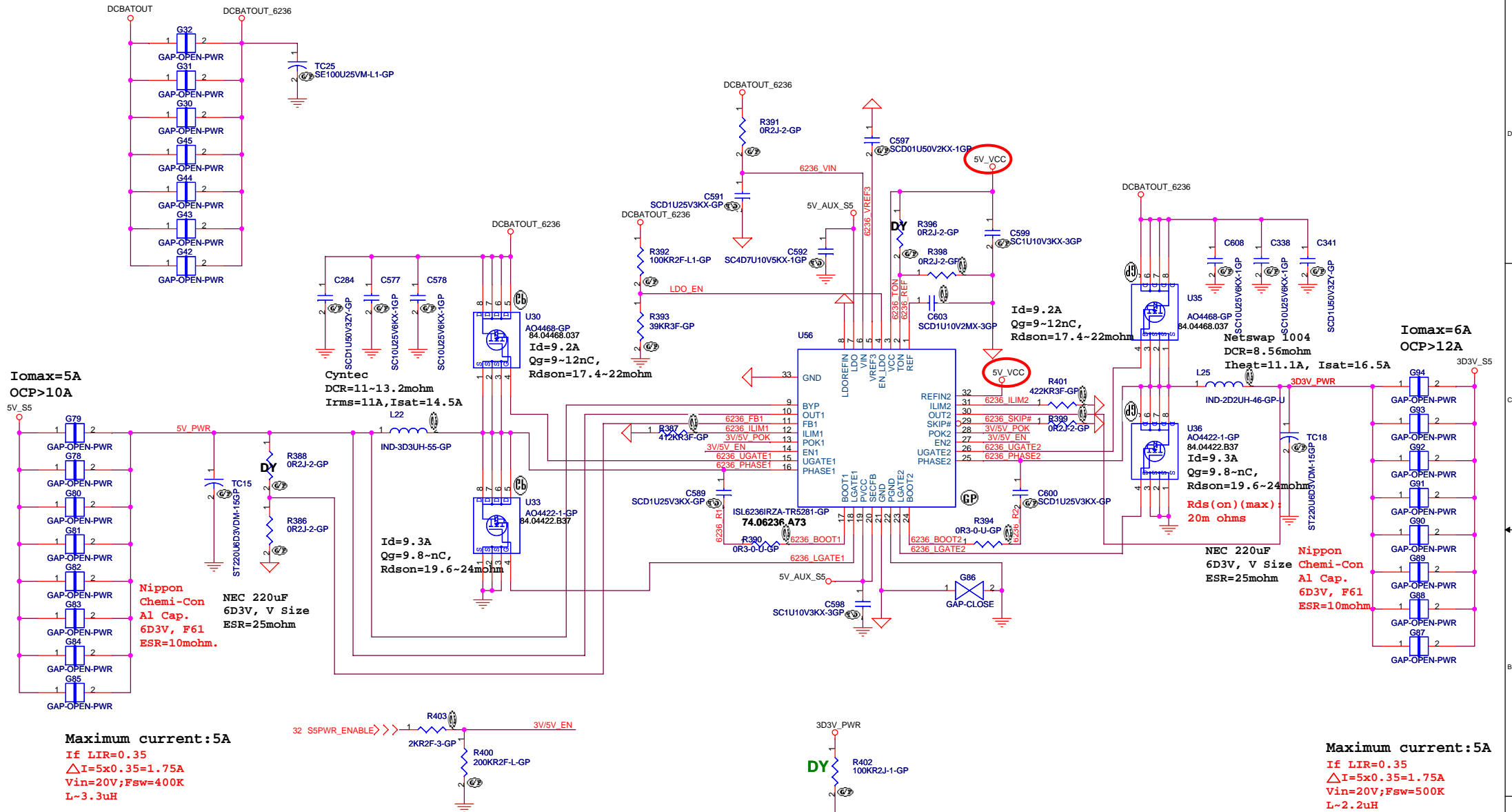


<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>AD/BATT CONN</b>
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<Core Design>

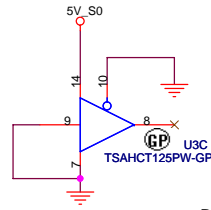
緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL6236 5V 3D3V		
Size	Document Number	Yukon	Rev
A3			SA
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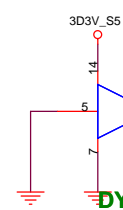




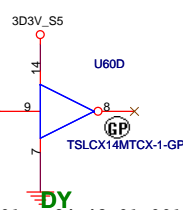




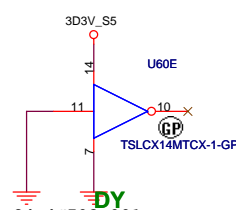
DUMMY in SA



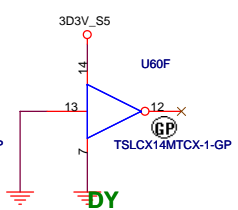
34.42Y01.001



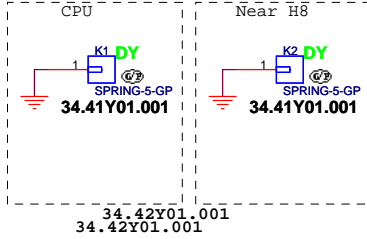
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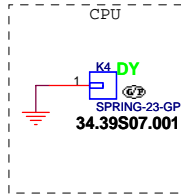
34.4G502.001



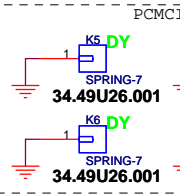
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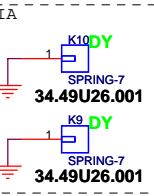
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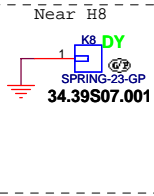
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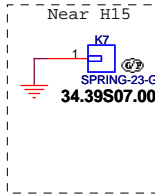
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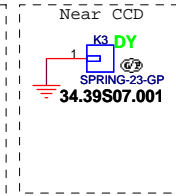
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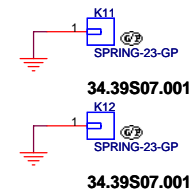
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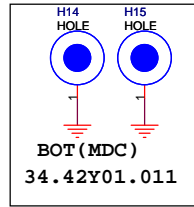
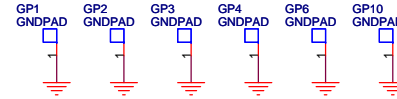
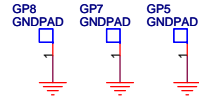
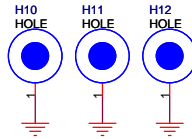
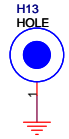
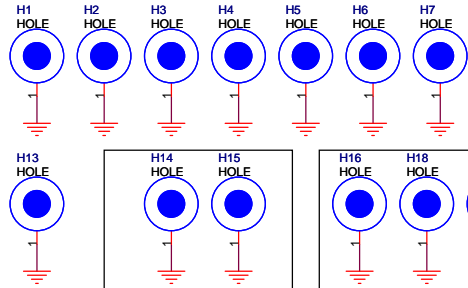
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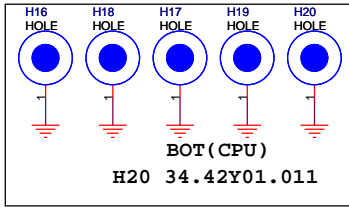
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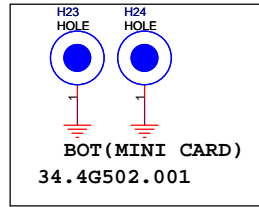
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34.39S07.001



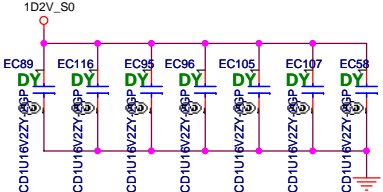
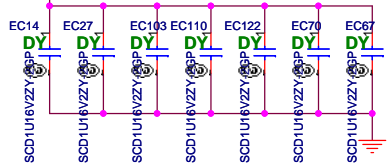
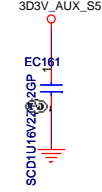
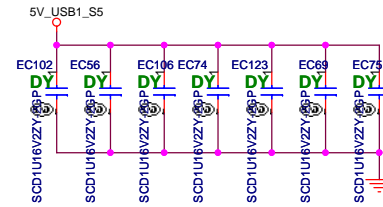
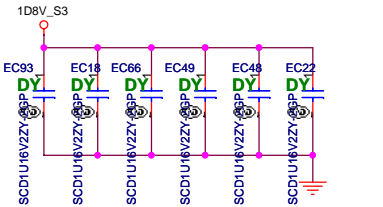
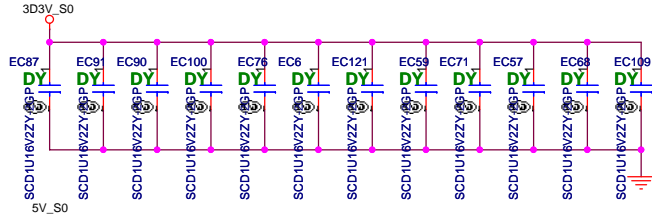
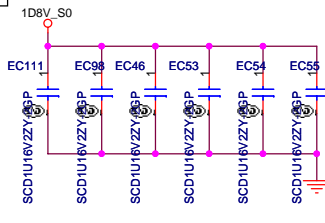
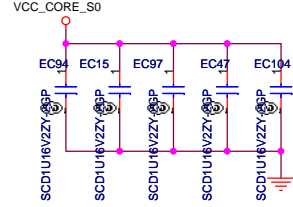
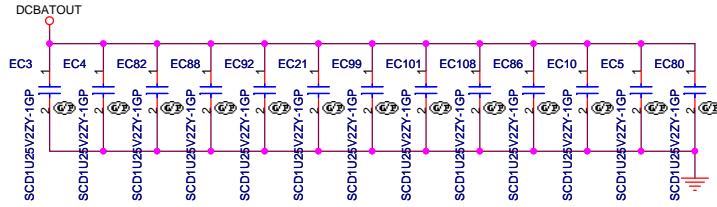
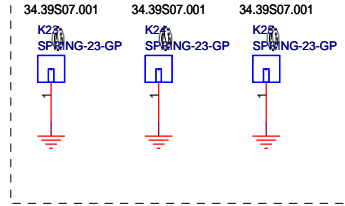
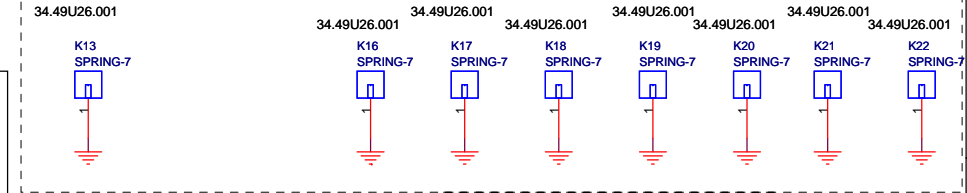
BOT (MDC)  
34.42Y01.011



BOT (CPU)  
H20 34.42Y01.011



BOT (MINI CARD)  
34.4G502.001



<Core Design>

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